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FUSION

(MS-7702L2 Ver:0A) mATX: 244mm * 244mm

CPU:

AMD FM1(Llano uPGA FAMILIES)

System Chipset:

AMD - Hudson D3/D2

On Board Chipset:

CLOCK GEN --FCH internal clock gen

LPC Super I/O --NCT6776F

LAN-Realtek 8111E/8105E

Azalia CODEC - Realtek ALC892/662/888/

Main Memory:

DDR III * 4 (max 32G)

Expansion Slots:

PCI Express X16 Slot * 1

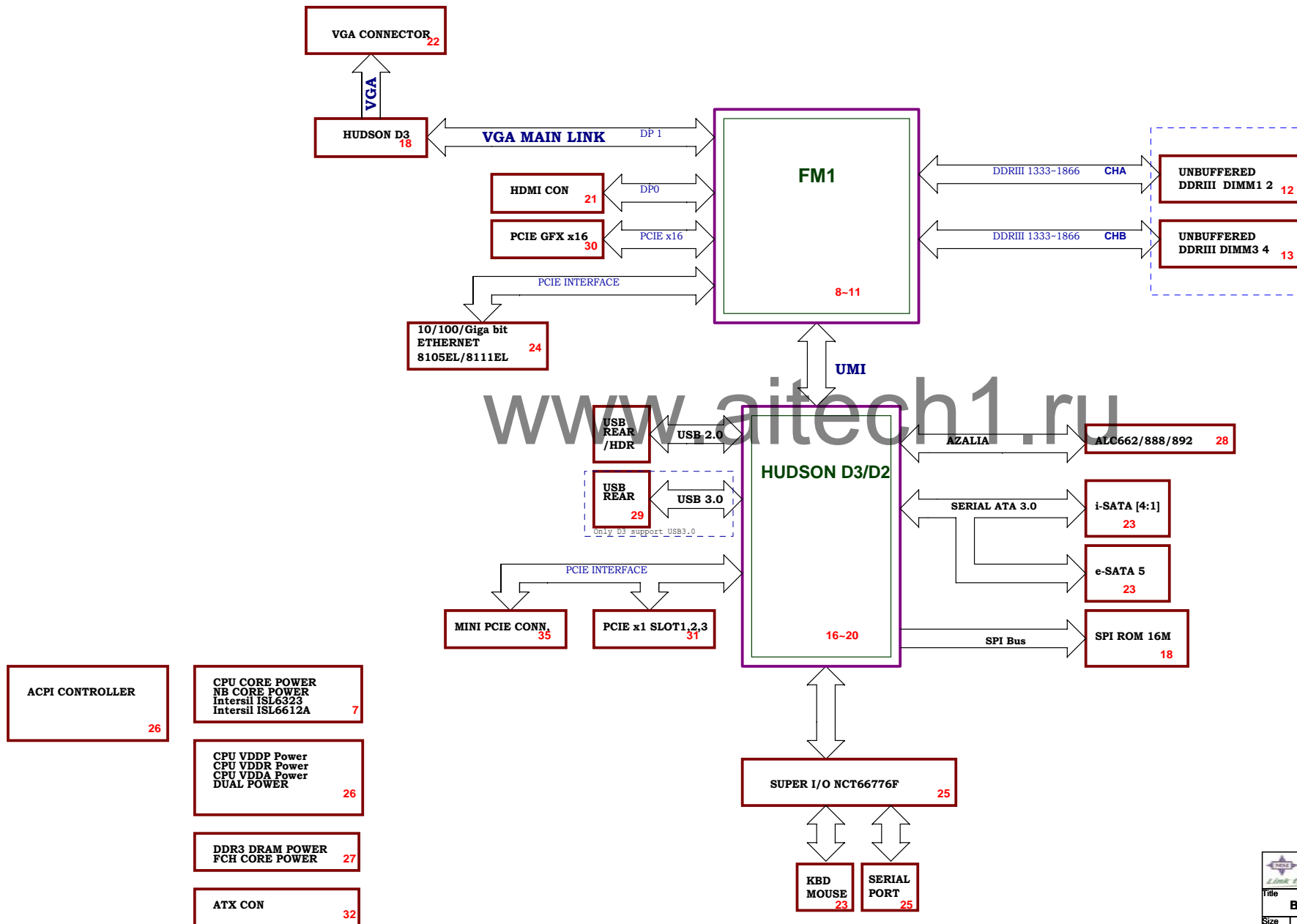
PCI Express X1 Slot * 3

MINI PCIE CONNECTOR *1

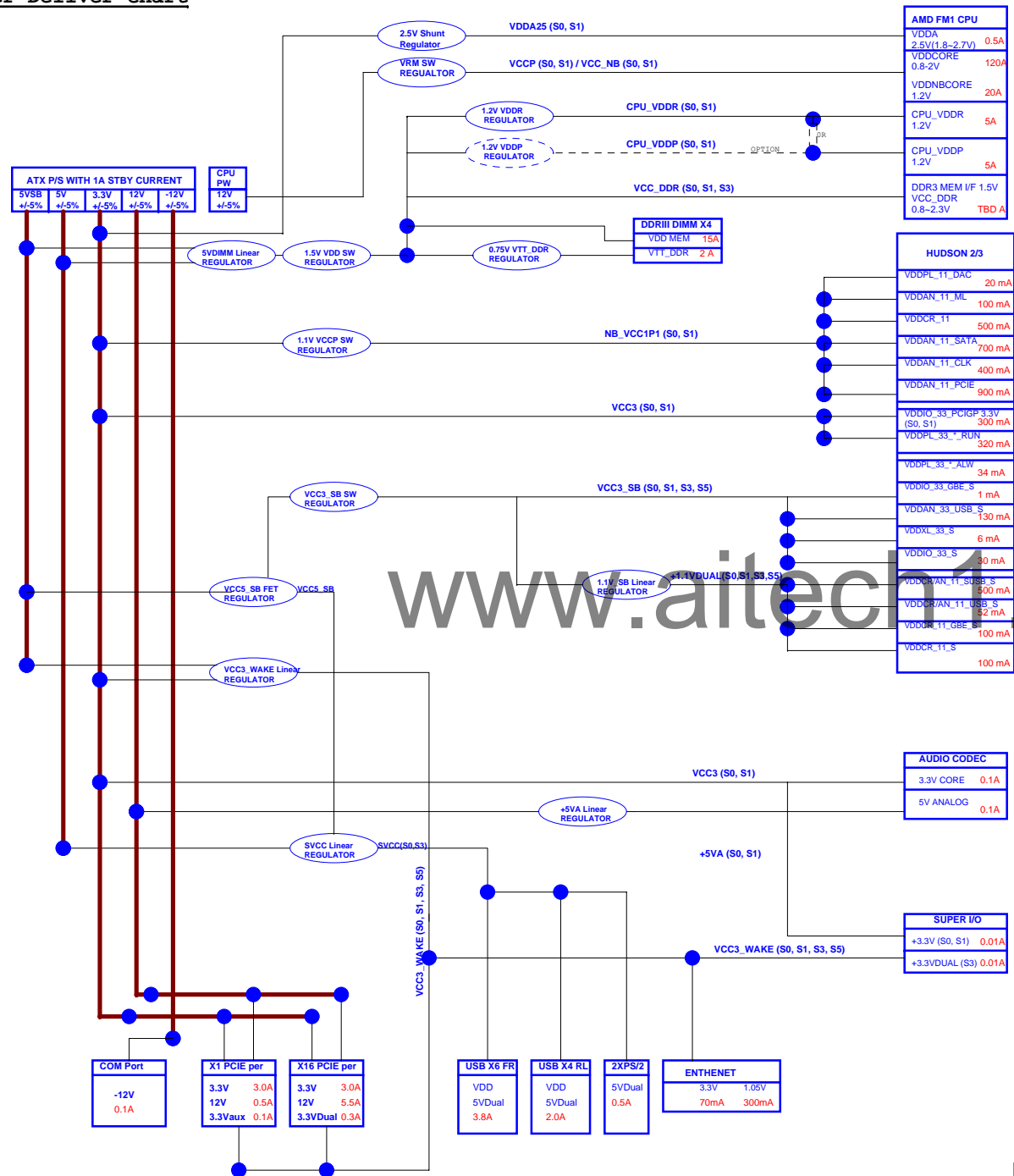
VRM

Controller - Intersil 6328 3+1 Phase

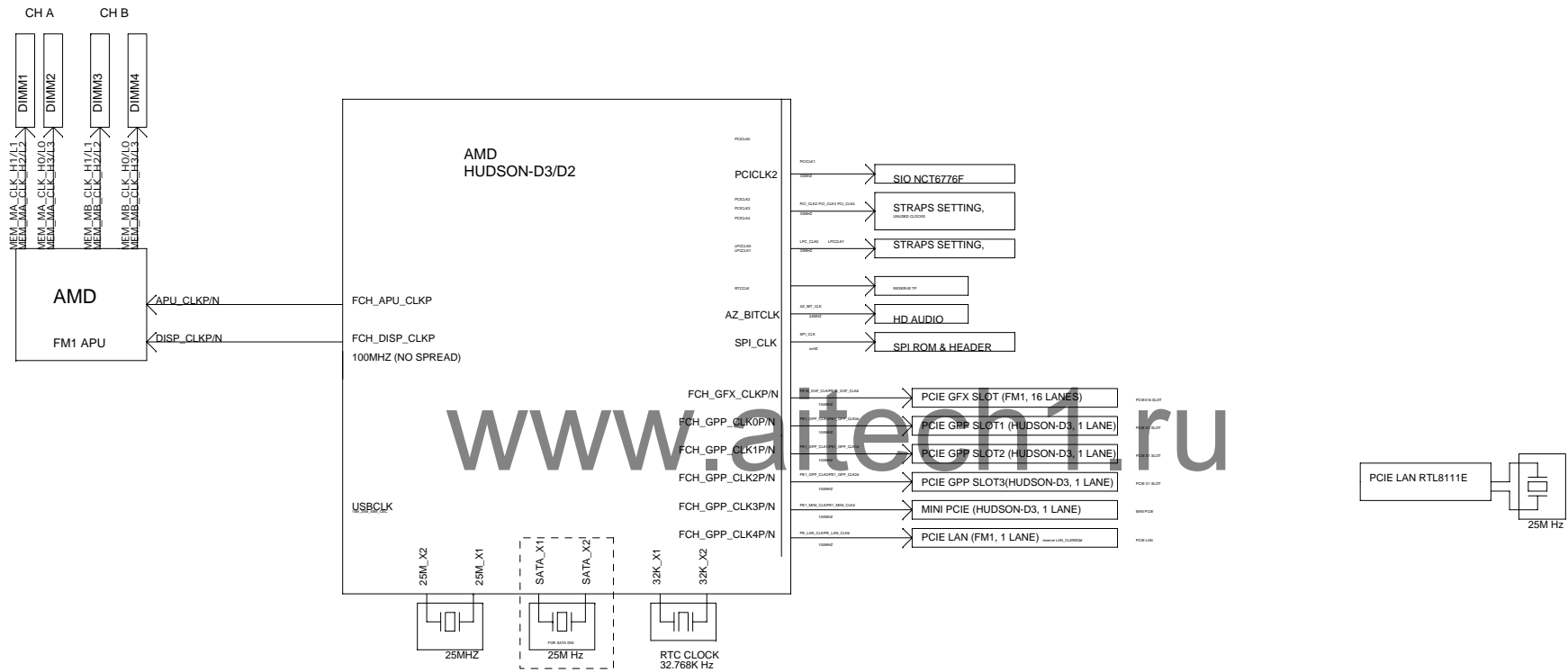
FUSION BLOCK DIAGRAM



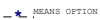
Power Deliver Chart



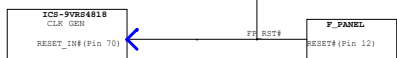
INTERNAL CLOCK MODE



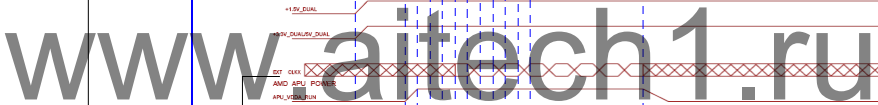
PWRGD MAP



RESET MAP



POWER ON SEQUENCE



SIO NCT6776F GPIO Config

Pin	GPIO	Power Rail	Function description	Comment
38	GP46	VSB	SIO_WAKE	
39	YLW_LED/GP45	VSB	SUS_LED	reserved
40	GRN_LED/GP44	VSB	PWR_LED	
42	GP67	VSB	USB_EN	OD
44	GP65	VSB	MB_ID0	GPI reserved
45	GP64	VSB	MB_ID1	GPI reserved
47	GP63	VSB	MB_ID2	GPI reserved
48	GP62	VSB	COM_GPIO2	GPI
49	GP61	VSB	CHASSIS_ID1	GPI reserved
50	GP60	VSB	CHASSIS_ID2	GPI reserved
78	GP36	VSB	SIO_VDUAL_EN	

FCH HUDSON D3/D2GPIO Config

Pin	pin Name	Function description
AJ3	AD0/GPIO0	CLEAR_CMOS
J2	IR_LED#/LLB#/GPIO184	MINI_PWRON
AD22	SATA_ACT#/GPIO67	SATA_LED#:SATA Channel Active
M6	TEMPIN3/TALERT#/GPIO174	FCH_TALERT#:Thermal Alert. The FCH can be programmed to generate an SMI, SCI, or IRQ13 through GPE, or generate an SMI without GPE in response to the signal's assertion.
V3	SPI_CLK/GPIO162	SPI Clock
V6	SPI_DI/GPIO164	SPI Data In
V5	SPI_DO/GPIO163	SPI Data Output
T6	SPI_CS1#/GPIO165	SPI Chip Select1#
V1	ROM_RST#/SPI_WP#/GPIO161	SPI write protect (active low)
Y6	SPI_HOLD#/GEVENT9#	SPI HOLD#. Assert low to hold the SPI transaction.
T8	USB_OC0#/SPI_TPM_CS#/TRST#/GEVENT12#	OC#0:USB 3.0 port 3,USB 2.0 port 13
J7	USB_OC1#/TDI/GEVENT13#	OC#1:USB2.0 port 4,5
P5	USB_OC2#/TCK/GEVENT14#	OC#2:USB2.0 port 8,9
P5	USB_OC3#/AC_PRES/TDO/GEVENT15#	OC#3:USB 3.0 port 0,USB 2.0 port 10
P6	USB_OC4#/IR_RX0/GEVENT16#	OC#4:USB 3.0 port 1,USB 2.0 port 11
T1	USB_OC5#/IR_TX0/GEVENT17#	OC#5:USB2.0 port 2,3
R8	USB_OC6#/IR_TX1/GEVENT6#	OC#6:USB2.0 port 0,1
M7	BLINK/USB_OC7#/GEVENT18#	OC#7:USB 3.0 port 2,USB 2.0 port12
	GPIO[171::173];GPIO[175::182];GPIO[193::194]	Configure as one of the following: 10-kΩ 5% pull-up resistor to +3.3V_S5. 10-kΩ 5% pull-down resistor.

DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1 CH-A	10100000B A0H	MEM_MA_CLK_H1/L1 MEM_MA_CLK_H2/L2
DIMM 2 CH-A	10100010B A4H	MEM_MA_CLK_H0/L0 MEM_MA_CLK_H3/L3
DIMM 3 CH-B	10100001B A2H	MEM_MB_CLK_H1/L1 MEM_MB_CLK_H2/L2
DIMM 4 CH-B	10100011B A6H	MEM_MB_CLK_H0/L0 MEM_MB_CLK_H3/L3

SMBus TABLE

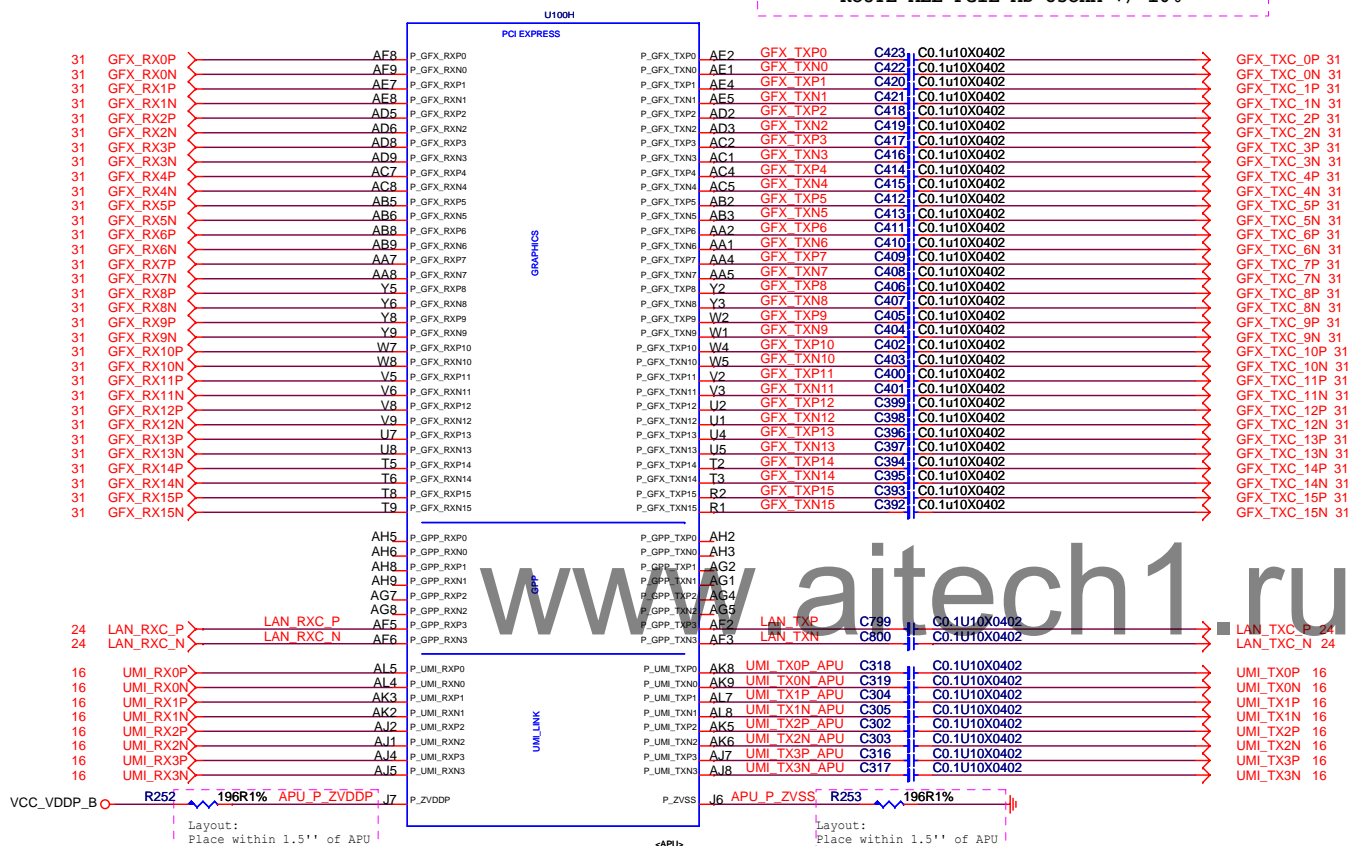
SOURCE	SINGLE NAME	LINKED DEVICE
APU	DPO_AUXP_C /DPO_AUXN_C	HDMI
	DP1_AUXP_C /DP1_AUXN_C	Hudson D2/3 DP to VGA translator
FCH	SCLK0/SDATA0	DIMMs,CLOCK GEN ,SIO
	SCLK1/SDATA1	LAN,PCIE SLOTS,MINI_PCIE
	SCLK3/SDATA3	TP

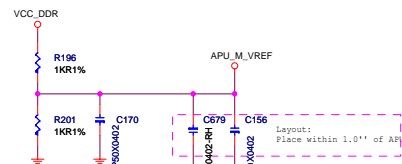
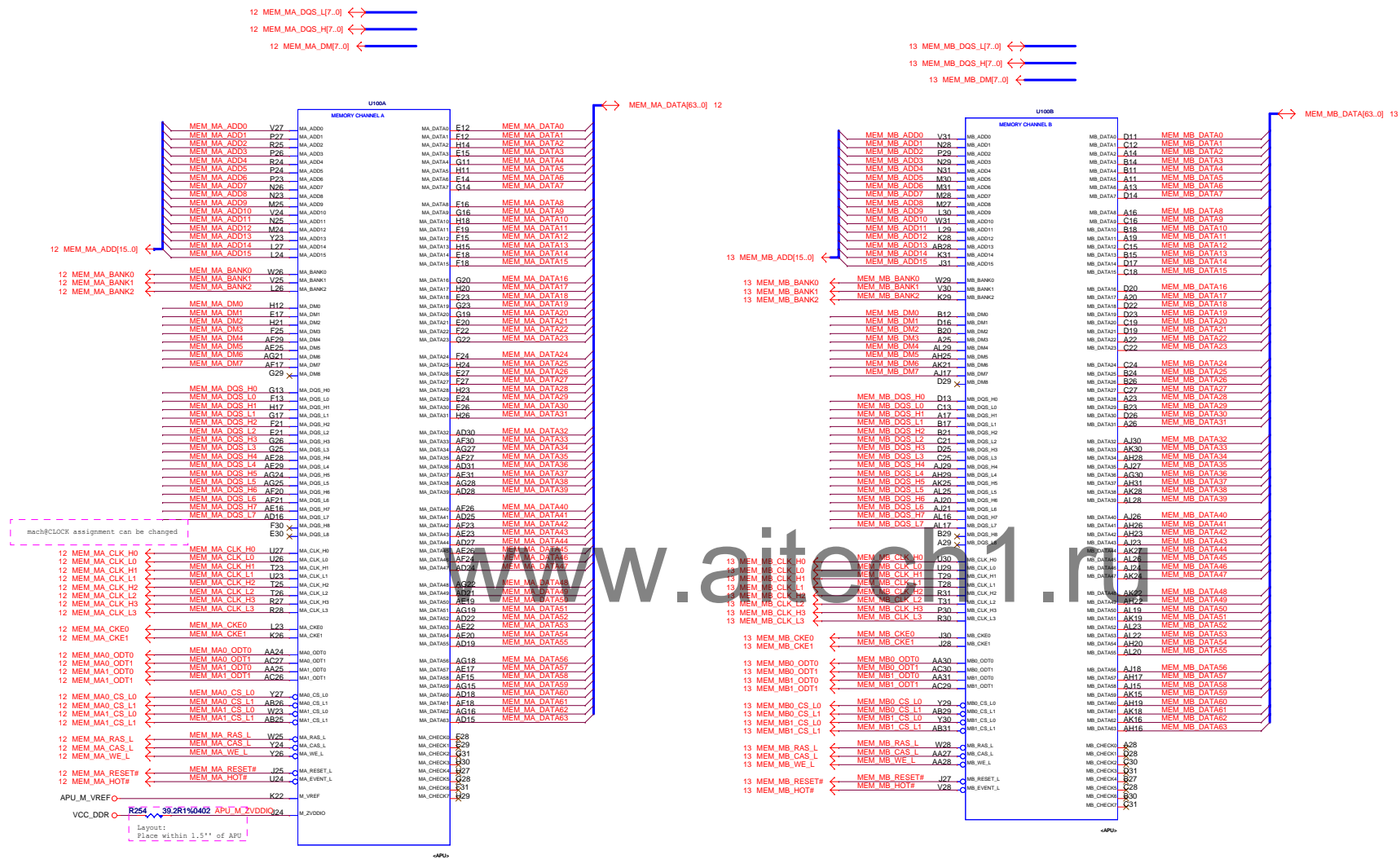
RESET TABLE

SOURCE	SINGLE NAME	LINKED DEVICE
FCH	PCIE_RST#	PCie 16X,1X,LAN,MINI_PCIE
	A_RST#	SIO,LPC debug
	PCIE_RST2#	RESERVE TP
	LDT_RST#	APU
	AZ_RST#	AZALIA CODEC
	DDR3_RST#	NC
	FC_RST#	DEBUG BUS
	ROM_RST#	NC
FRONT PANEL	FP_RST#	FCH,CLOCK GEN

FM1 PCIE I/F

mach@CRB PCIE AC Capacitors:75nF to 200nF
Layout: PLACE CAPS WITH APU < 1 INCH
ROUTE ALL PCIE AS 850HM +/-10%

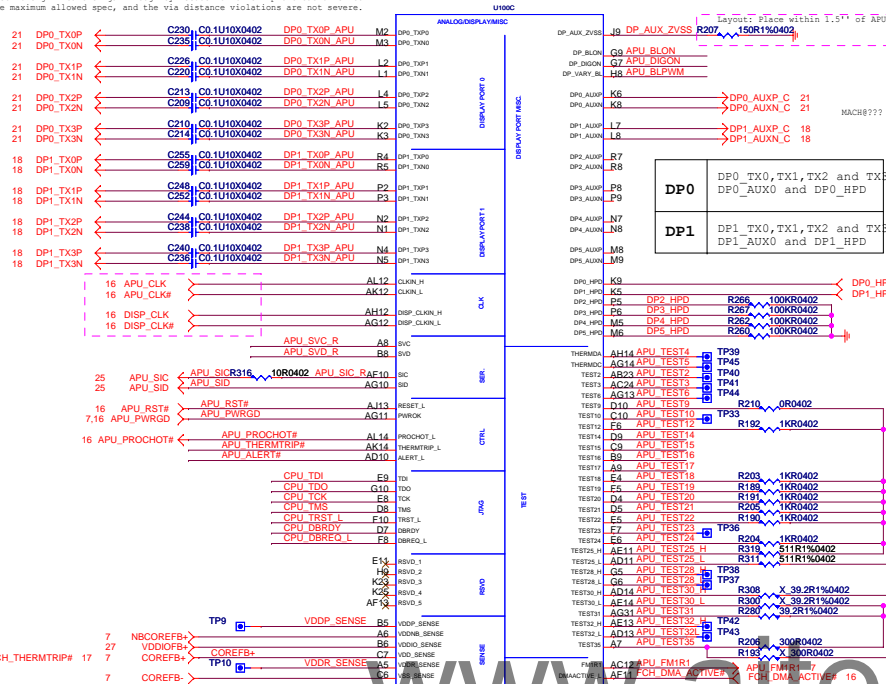




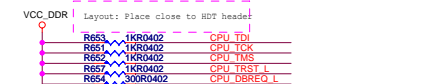
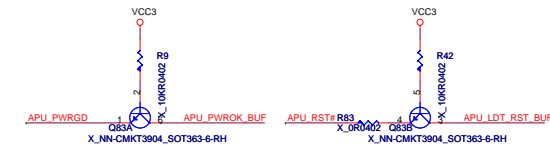
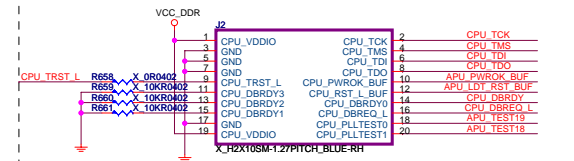
FM1 DISPLAY I/F

Note: Several vias on the DP0 interface violate the minimum distance rules for via to via spacing between diff pairs. These violations have been reviewed and approved on an individual basis, and pose no significant signal integrity issues for this implementation since the route lengths are under the maximum allowed spec, and the via distance violations are not severe.

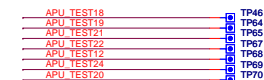
ROUTE PCIE AS 850MH +/-10%
PLACE CAPS WITH APU < 1 INCH
Trace length within 10"



HDT+ Connector



SCAN Conn,



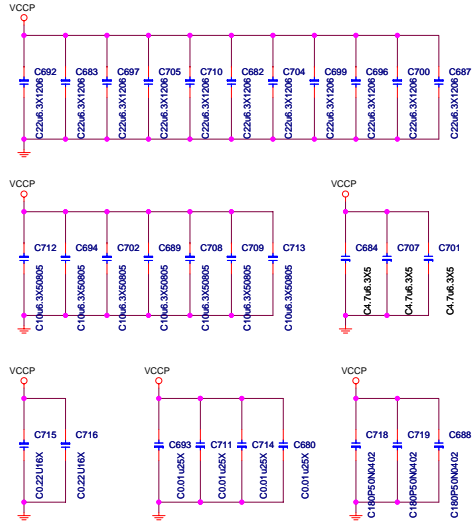
WARM RESET



GPU DEBUG



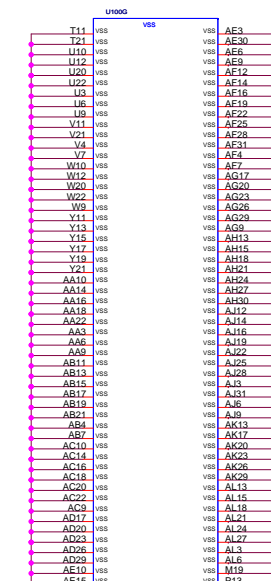
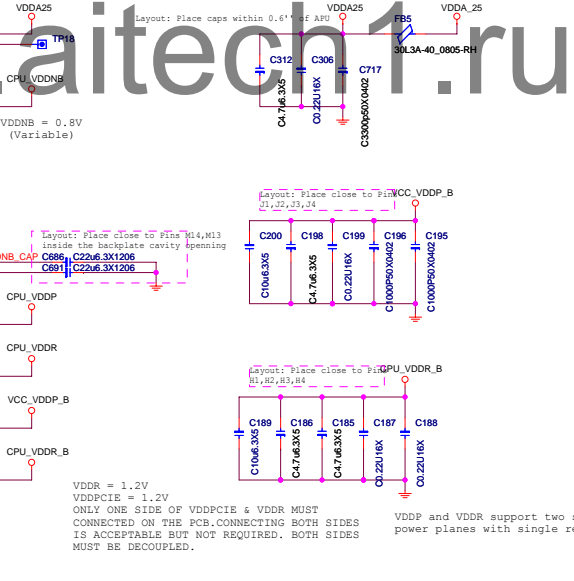
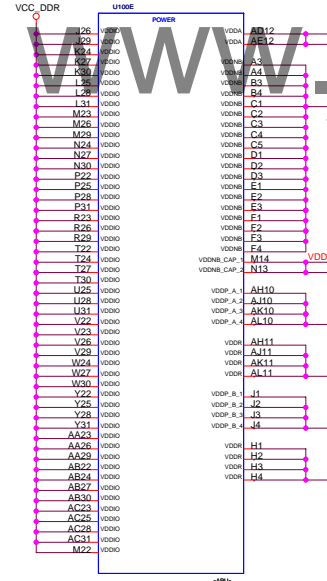
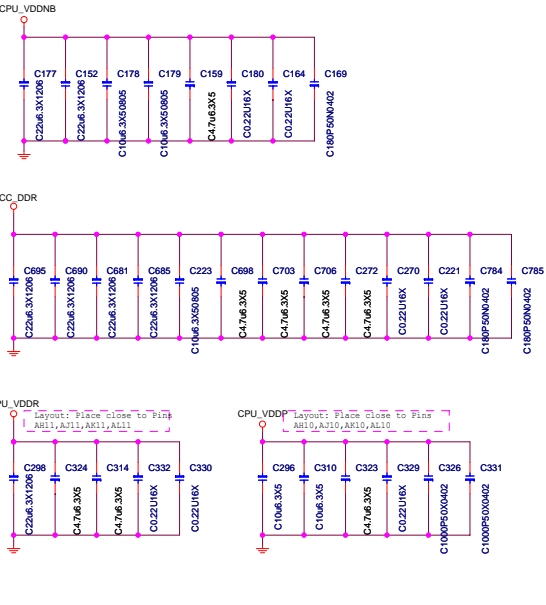
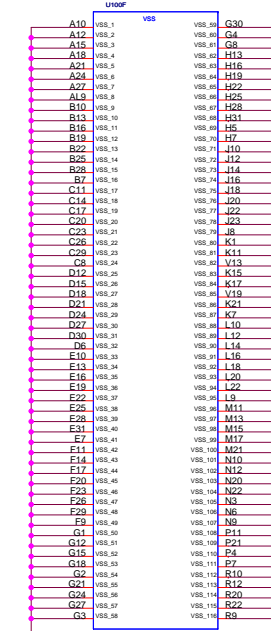
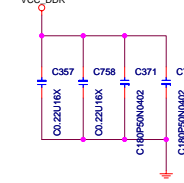
BOTTOM SIDE DECOUPLING



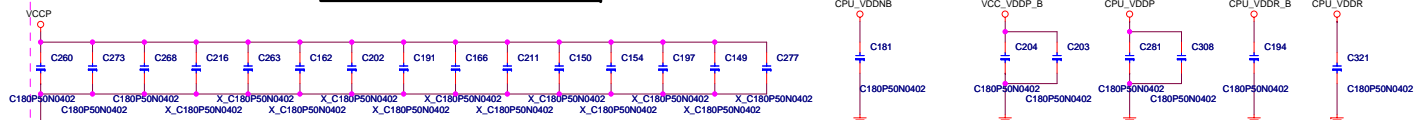
FM1 DECOUPLING CAPS

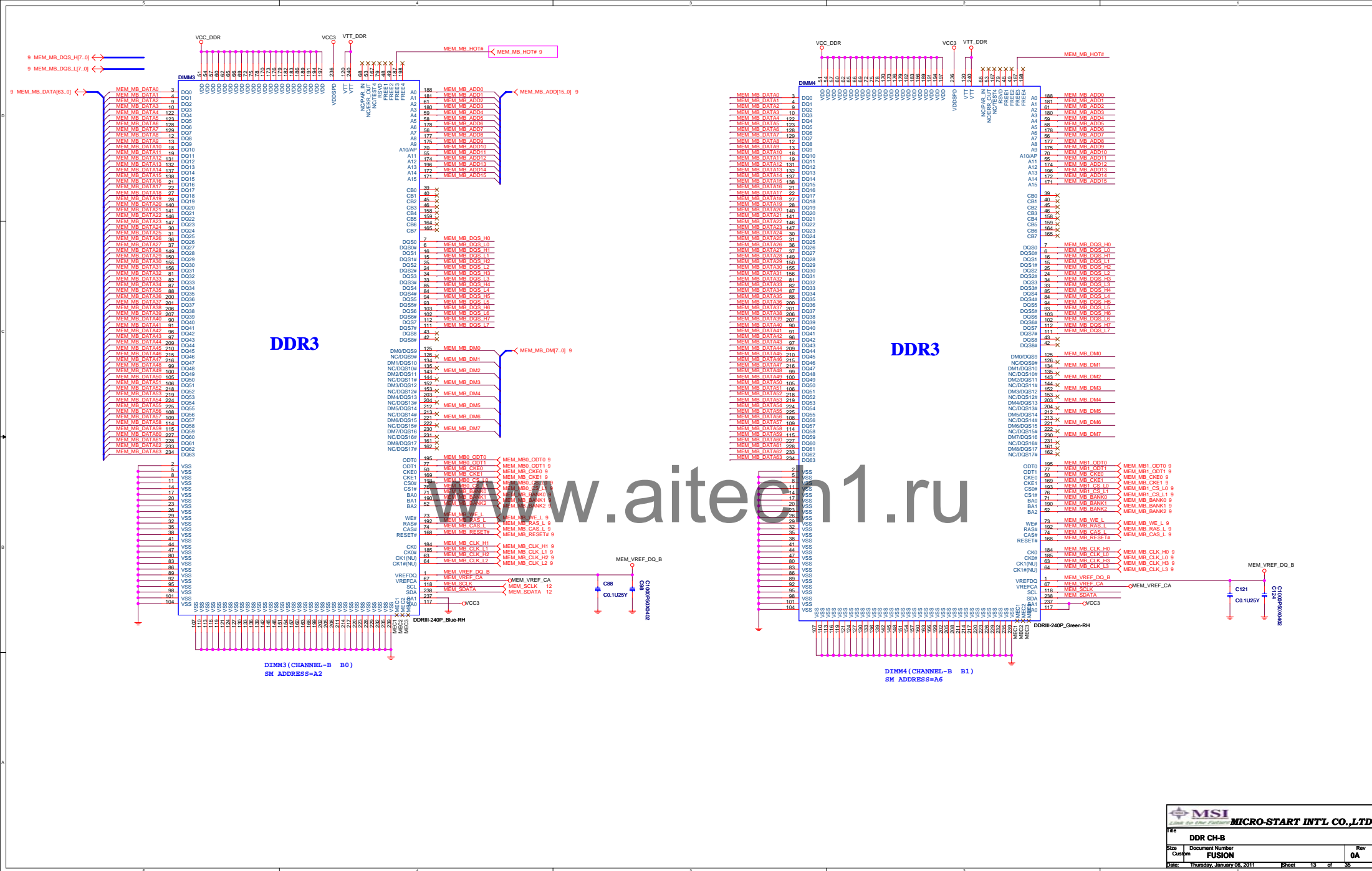
TOTLE POWER PINS	VSS	VDD	VDDNB	VDDIO	VDDP	VDDR	VDDA	Mref
416	226	102	19	51	8	8	4	2
VALUE/SIZE/ MATERIAL	COMB	COMB	SPLIT	SPLIT				
220/1206/X5R	/	11	2	4	/	1	/	/
100/0805/X5R	/	7	2	1	2+1(B)	1	/	/
4.70/0805/X5R	/	3	1	4	2	2+2	2	1
0.220/0603/X5R	/	2	2	2+2	2	2	2	1
0.10/0603/X5R	/	/	/	/	/	/	/	1
0.010/0603/X5R	/	4	/	/	/	/	/	/
3.3 nF/0603/X5R	/	/	/	/	/	/	/	1
1 nF/0603/X5R	/	/	/	/	/	/	/	1
1 nF/0603/X5R	/	/	/	/	4	/	/	/
180 pF/0603/X5R	/	3	1	2+2	2	/	/	/

Place across each VDDIO-GND plane seam

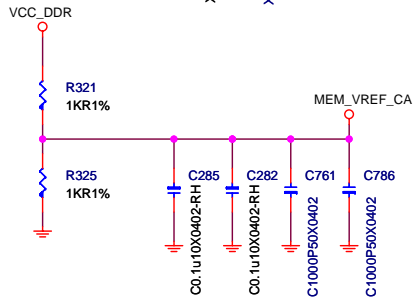
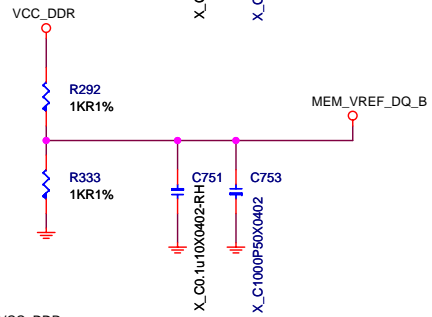
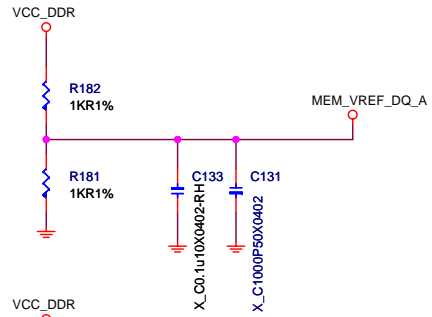


EMC Caps On Bottom side



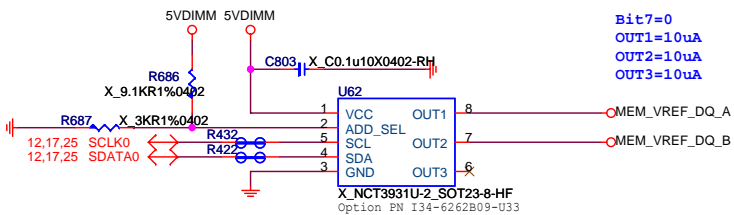


DDR REF POWER & CAPS

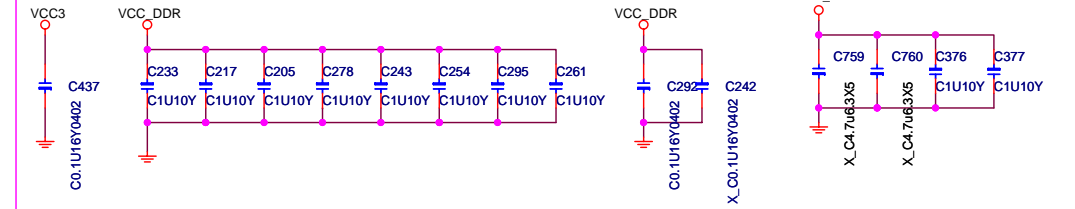


VOLTAGE CONSOLE

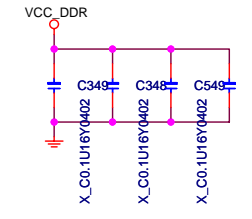
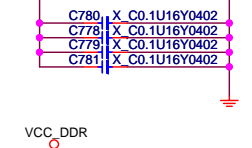
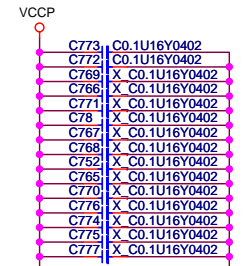
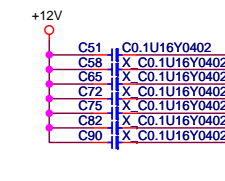
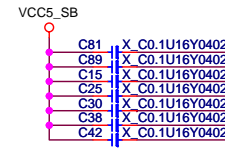
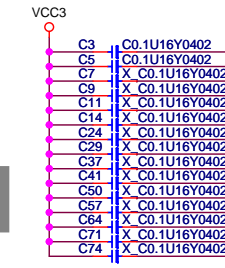
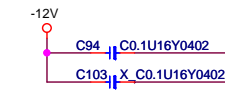
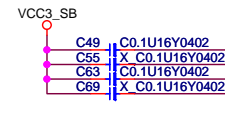
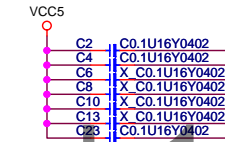
0x28:RH=9.1K,RL=3K;Bit7=0




De-coupling Caps For DIMMs

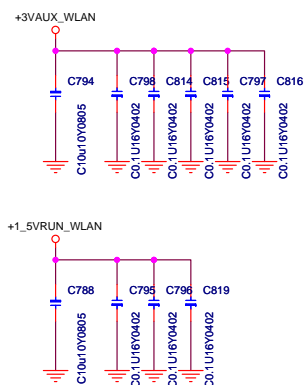
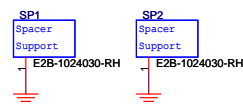
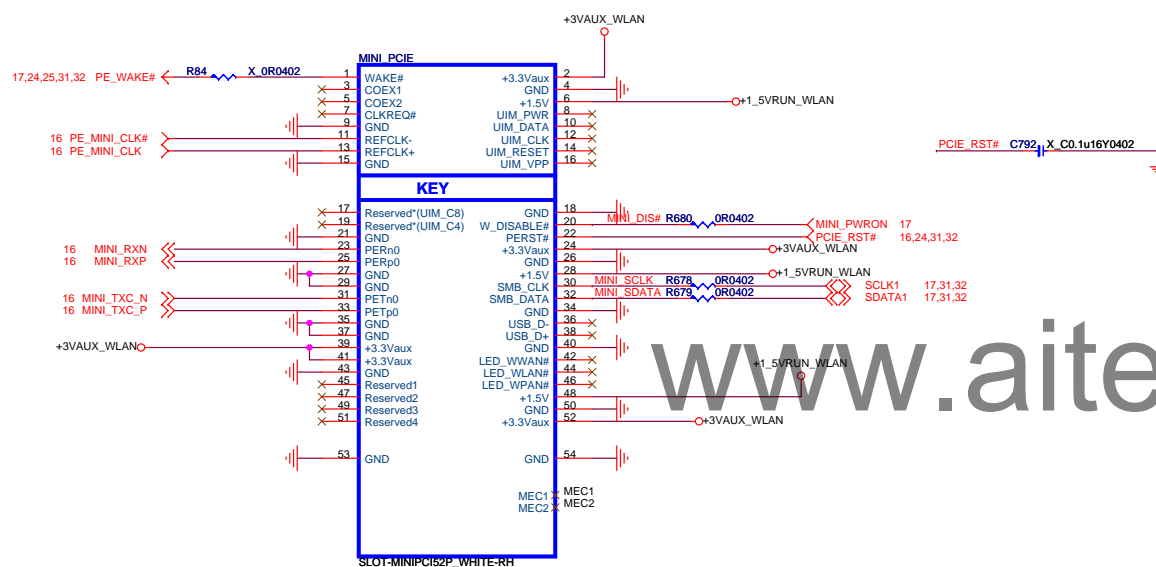


EMI Reserved

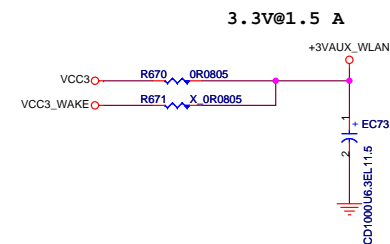
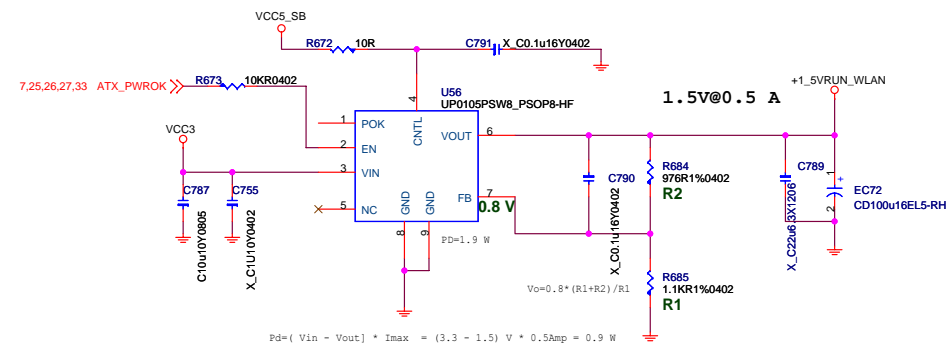


 MICRO-START INT'L CO.,LTD.		
Title		
DDR REF POWER & CAPS		
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Date:	Thursday, January 06, 2011	Sheet 14 of 35

MINI PCIE CONN,



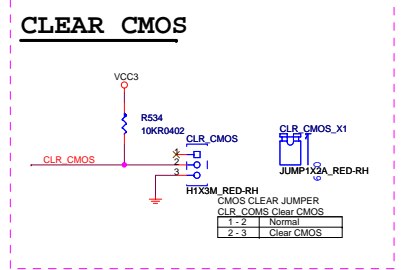
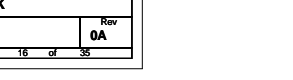
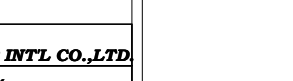
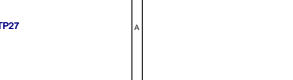
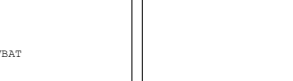
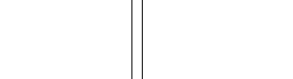
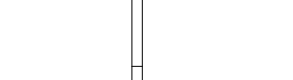
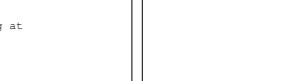
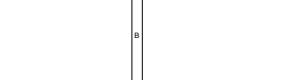
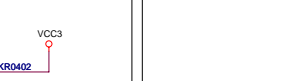
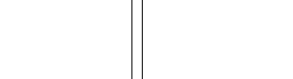
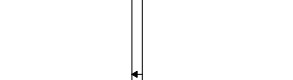
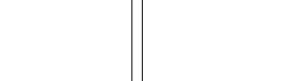
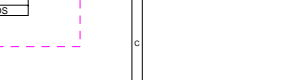
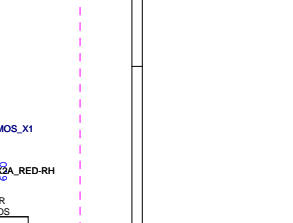
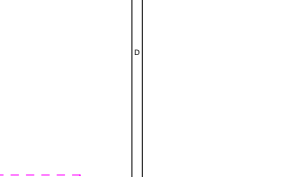
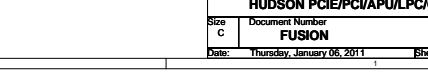
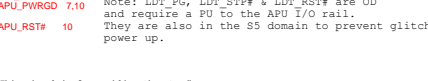
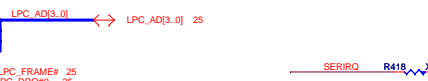
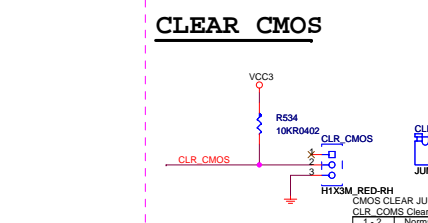
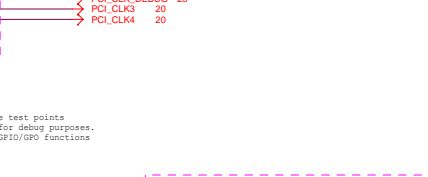
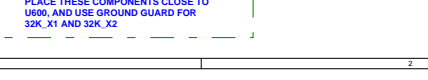
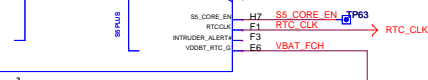
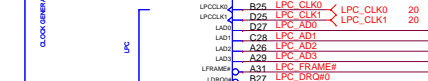
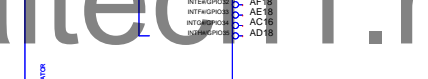
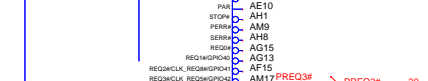
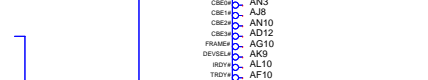
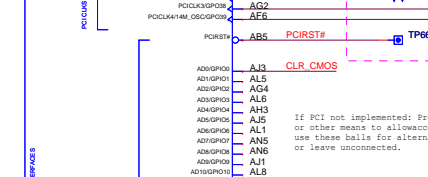
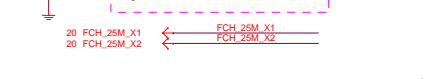
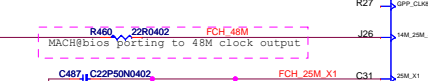
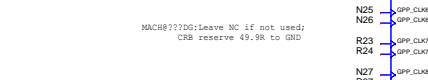
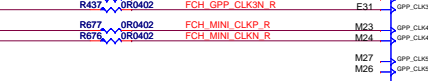
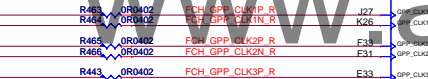
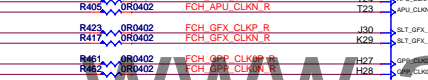
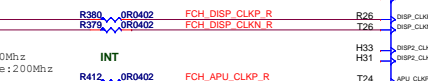
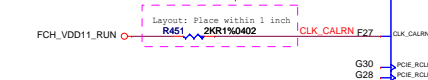
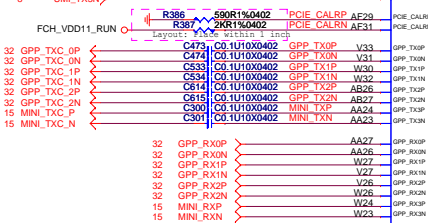
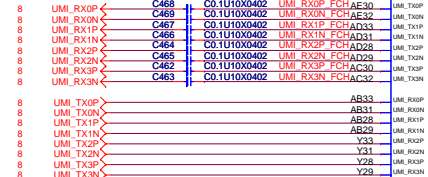
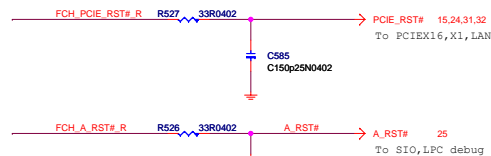
+1_5VRUN_WLAN POWER



A screenshot of a Wi-Fi network scan interface. The top part shows a list of detected networks. The first network is 'www.aitech1.ru' with a signal strength of -15 dBm. Below this, there is a detailed view of the selected network, showing its name, signal strength, and other details. The signal strength is highlighted in red.

HUDSON PCIE/PCI/APU/LPC/CLK

A_RST# for LPC device;
PCIE_RST# for APU PCIE device;
PCIE_RST#2 FCH PCIE device



Note: LDT_PG, LDT_STP# & LDT_RST# are OD and require a PU to the APU I/O rail. They are also in the S5 domain to prevent glitching at power up.

This signal is for enabling the standby power when S5 plus logic is enabled.

Layout: VBAT route 20mil

FCH 50KR internal PU to VBAT

RTC_CLK TP27

Layout: Place close to pin B1 ASAP 0603 size and XSR for CMOS issue

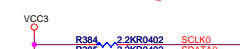
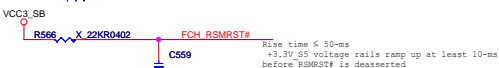
Layout: Place within 1.3 inch of FCH

Layout: Place within 1.3 inch of FCH

HUDSON ACPI/USB/AZ/GPIO



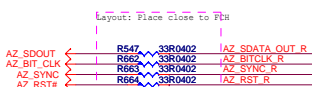
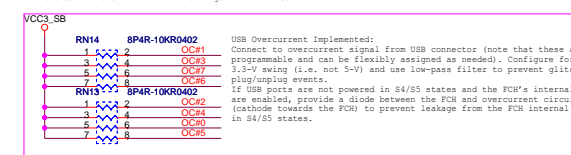
Layout: Place close to FCH ASAP
FCH_PWRGD C595.X C1000P50X0402



+3Vaux_WLAN

R681 **10K R0402** **MINI PWRON**

A pull-up resistor between W_DISABLE# and +3.3Vaux is required on the card and should be in the range of 100 kΩ to 200 kΩ.



R550 may stuff 15pF cap for EMI



mach@Rerouting the USB pairs follow layout

USB11	FRONT PANEL
USB10	FRONT PANEL
USB9	FRONT PANEL
USB8	FRONT PANEL
USB7	FRONT PANEL
USB6	FRONT PANEL

USB3	USB2 BOTTOM
USB2	USB2 TOP
USB1	LAN USB BOTTOM
USB0	LAN USB TOP

FCH_VDD_11_SSUSB_S

FOR Pin H19,G19
Use as GPIO or configure as one of
the following:
10-kΩ 5% pull-up resistor to +3.3V_S5
10-kΩ 5% pull-down resistor.

→ FCH_GPIO199 20

able function

Wake On Modem Header

	N_RI	RI#
Active	+12V	Low
Normal	-12V	High



Layout: Place within 1" of FCU

R386 1KR1Y0402 SATA_CALRP AF28
R389 1KR1Y0402 SATA_CALRN AF27

SATA_LED# ← SATA_LED# AD22

SATA_ACTINGPROPR

X06 X_C22P50N040

FCH_SATA_X1 AF21

SATA_X1

MACH0 ???

Y4
X_25MHZ18P_0

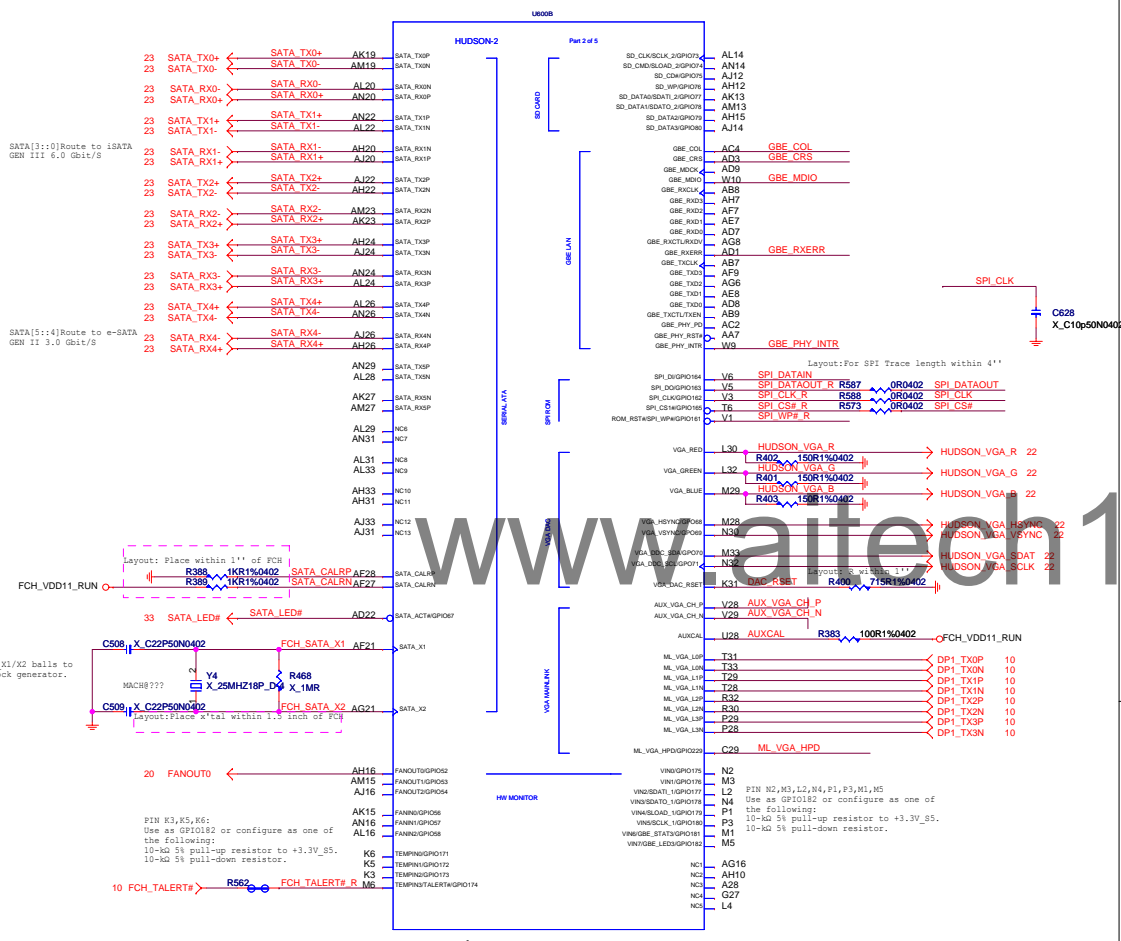
R468
X_1MR

X09 X_C22P50N040

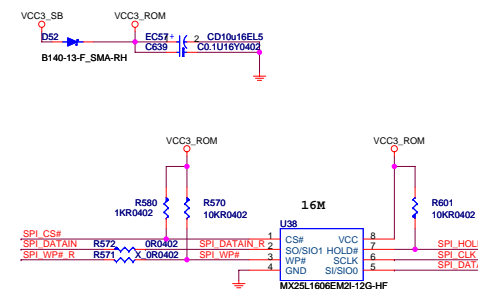
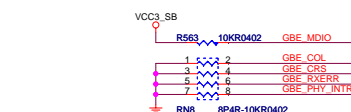
FCH_SATA_X2 AG21

SATA_X2

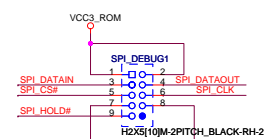
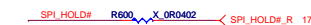
Layout: Place x4 times within 1 inch of FCU



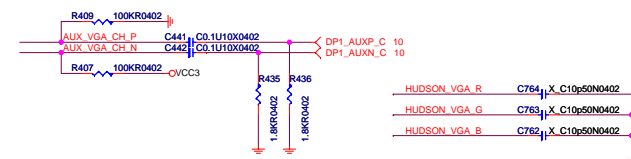
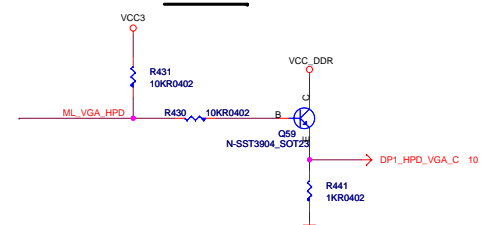
SPI ROM & DEBUG HEADER



MACH@Reserve OR serial registers for
SI overshoot/undershoot debug

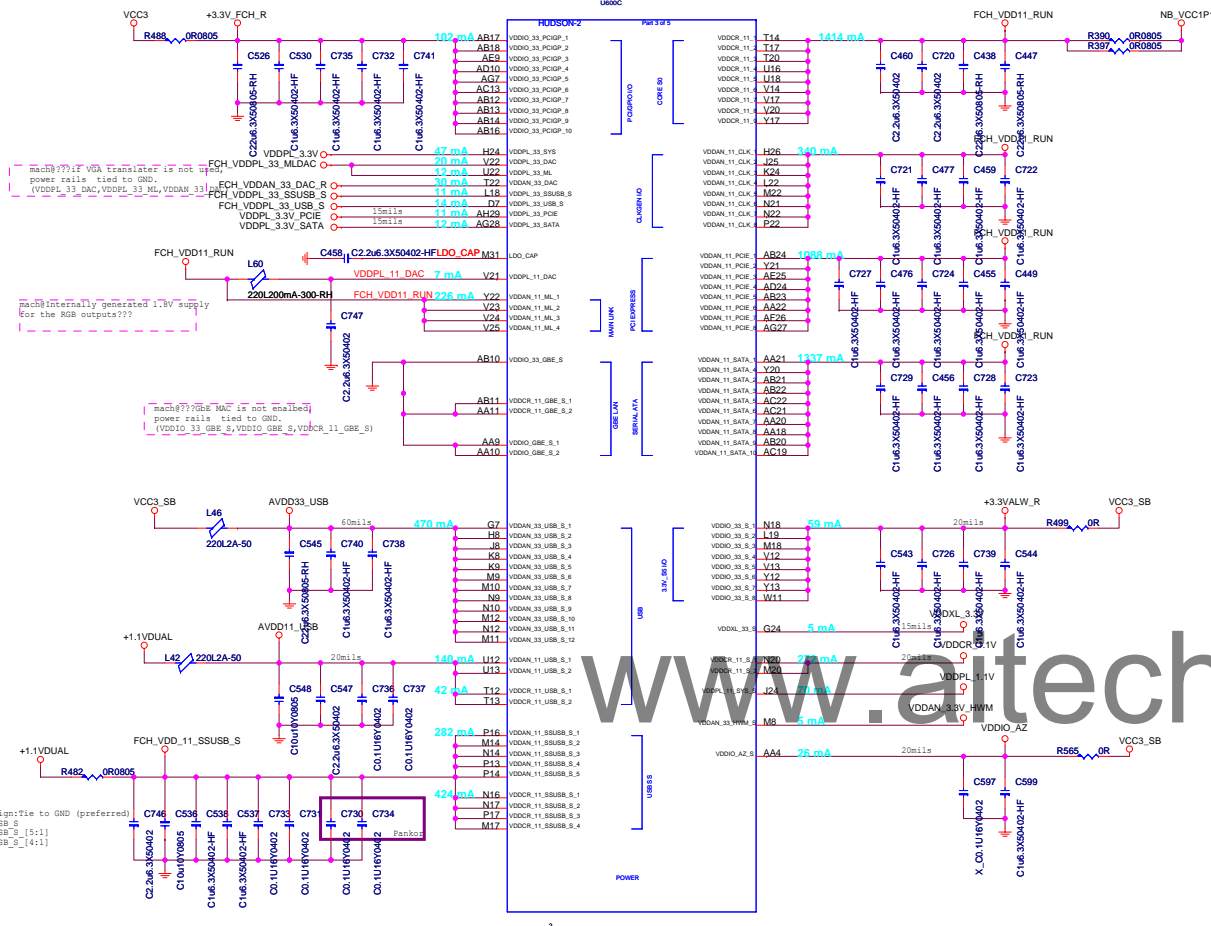


VGA HPD

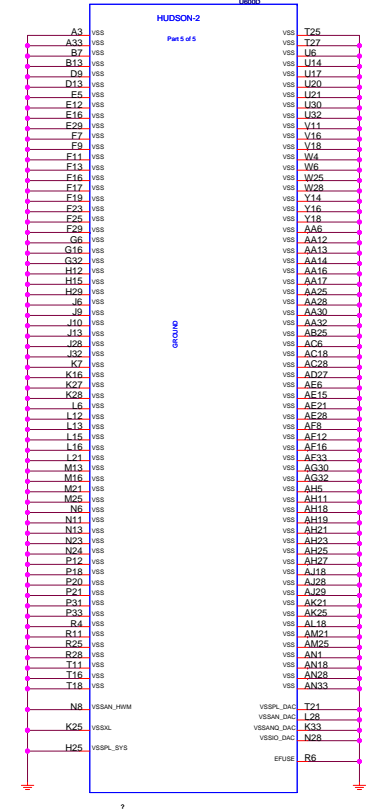


HUDSON POWER&DECOUPLING

Connected directly to the power plane with width > 100 mils with area fill under the FCH.

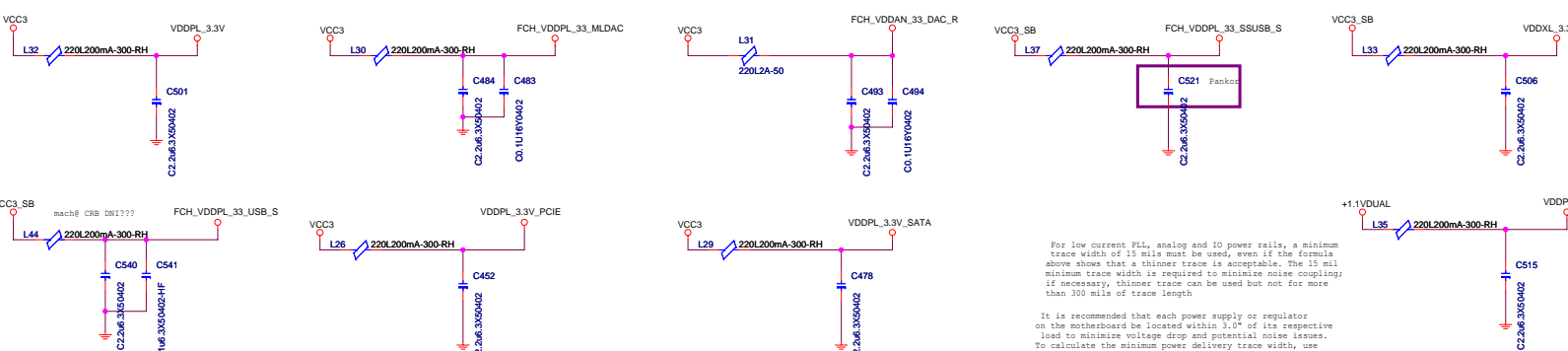


Power Rails	Hudson D3	Hudson D2
NB_VCC1P1	max 4412 mA	
VDDCR_11 [9:1]	1120 mA	1414 mA
VDDAN_11_CLK [8:1]	340 mA	
VDDAN_11_PCIE [8:1]	1088 mA	
VDDAN_11_SATA [10:1]	1337 mA	
VDDAN_11_ML [4:1]	226 mA	
VDDPL_11_DAC	7 mA	
VCC3	max 319 mA	
VDDIO_33_PCIGP [10:1]	102 mA	
VDDPL_33_SYS	47 mA	
VDDPL_33_DAC	20 mA	
VDDPL_33_ML	12 mA	
VDDPL_33_PCIE	11 mA	
VDDAN_33_DAC	30 mA	
VCC3_SB	max 659 mA	
VDDIO_33_S [8:1]	59 mA	
VDDIO_AZ_S	26 mA	
VDDXL_33_S	5 mA	
VDDAN_33_HWM_S	12 mA	
VDDIO_GBE_S [2:1]	145 mA GND	
VDDIO_33_GBE_S	2 mA GND	
VDDPL_33_USB_S	14 mA	
VDDAN_33_USB_S [12:1]	470 mA	
VDDPL_33_SSUSB_S	11 mA	0 mA
+1.1VDUAL	max 1293 mA	
VDDCR_11_SYS_S [2:1]	272 mA	
VDDCR_11_GBE_S [2:1]	63 mA GND	
VDDPL_11_SYS_S	70 mA	
VDDAN_11_USB_S [2:1]	140 mA	
VDDCR_11_USB_S [2:1]	42 mA	
VDDAN_11_SSUSB_S	5282 mA	0 mA
VDDCR_11_SSUSB_S [4:2]	42 mA	0 mA



Layout:
VSSPL_SYS,VSSAN_HWM CONNECT TO GND
WITH A SEPARATED VIA

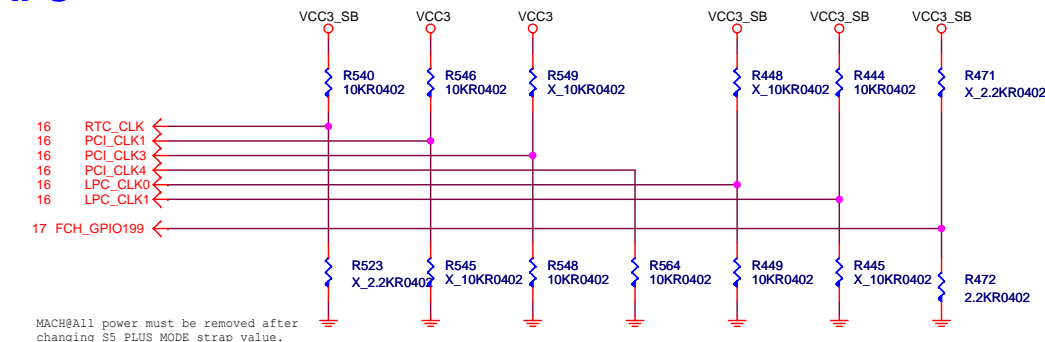
LAYOUT:
ROUTE THE POWER TRACES 15MILS WIDTH AT LEAST
PLACE THE DECOUPLING CAPS CLOSE TO FCH ASAP
PLACE FB<1", CAPS <0.2"



For low current PLL, analog and IO power rails, a minimum trace width of 15 mils must be used, even if the formula above shows that a thinner trace is acceptable. The 15 mil minimum trace width is required to minimize noise coupling; if necessary, thinner trace can be used but not for more than 300 mils of trace length.

It is recommended that each power supply or regulator on the motherboard be located within 3/8" of its respective load to minimize voltage drop and potential noise issues. To calculate the minimum power delivery trace width, use the formula: $V_{drop} = I \cdot R$, where $R = \rho \cdot L / A$ (ρ = resistivity of material, L = trace length, A = trace cross-sectional area). V_{drop} must be < 2.5% of the nominal power rail voltage under maximum current conditions

FCH REQUIRED STRAPS



	RTCCLK	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO199
PULL HIGH	S5 PLUS MODE DISABLED DEFAULT	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	Reserved	EC ENABLED	INTERNAL CLOCK GEN ENABLED DEFAULT	LPC ROM
PULL LOW	S5 PLUS MODE ENABLED	FORCE PCIE GEN1	IGNORE DEBUG STRAPS DEFAULT	Required setting for intergrated CLOCK MODE DEFAULT	EC DISABLED DEFAULT	INTERNAL CLOCK GEN DISABLED	SPI ROM DEFAULT

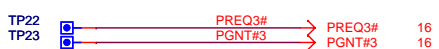
FCH DEBUG STRAPS

Provided test point access for lab use.
FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

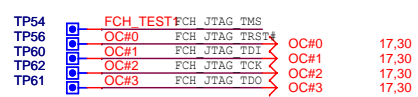


	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	RESERVED	Normal REFCLK Termination DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL DOWN	BYPASS PCI PLL	RESERVED	Inverted REFCLK Termination	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

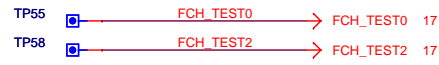
FCH PCIE EEPROM STRAPS



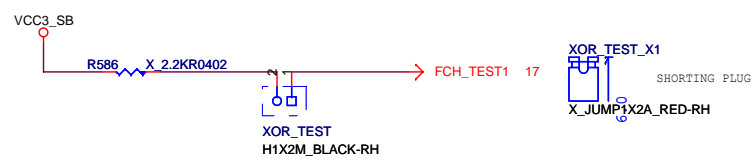
FCH ICE DEBUG /JTAG TEST PINS




FCH XOR CHAIN TEST



FEST2	FEST1	FEST0	Description
0	1	X	Enable test mode





Link to the Future

MICRO-START INT'L CO.,LTD.

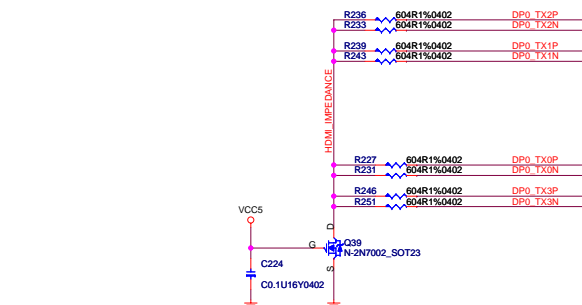
Title
HUDSON STRAPS

Size B Document Number
FUSION

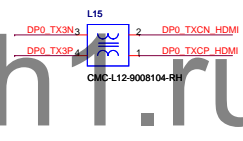
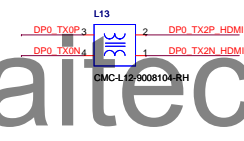
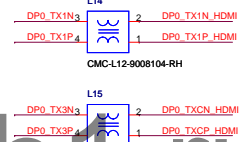
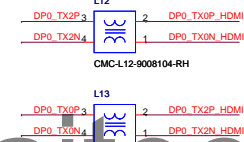
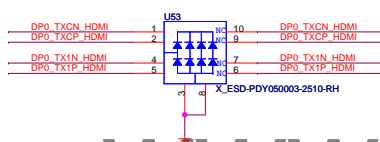
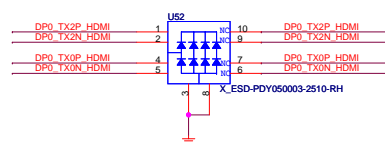
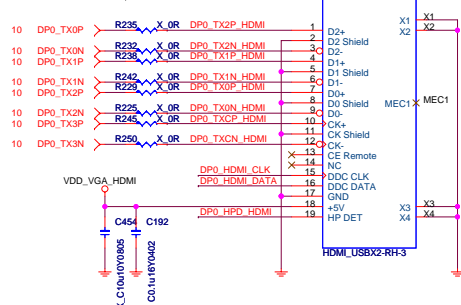
Date: Thursday, January 06, 2011 Sheet 20 of 35

Rev
0A

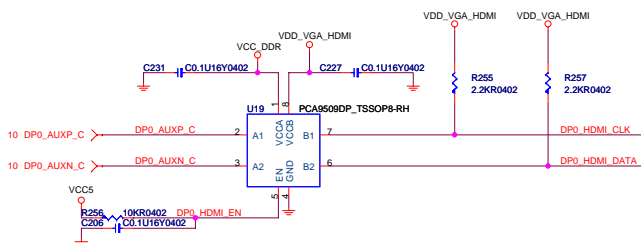
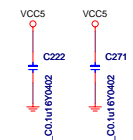
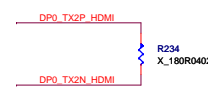
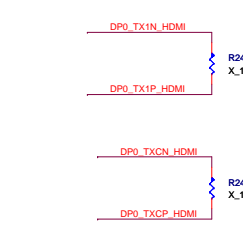
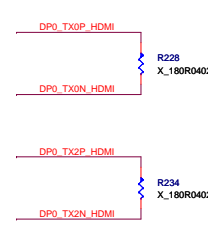
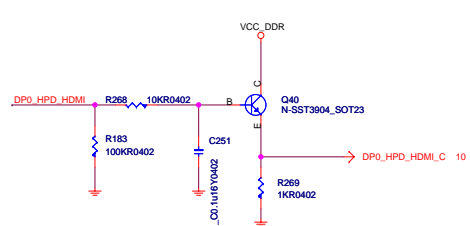
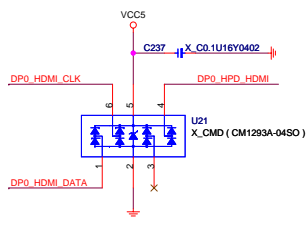
HDMI CONN,



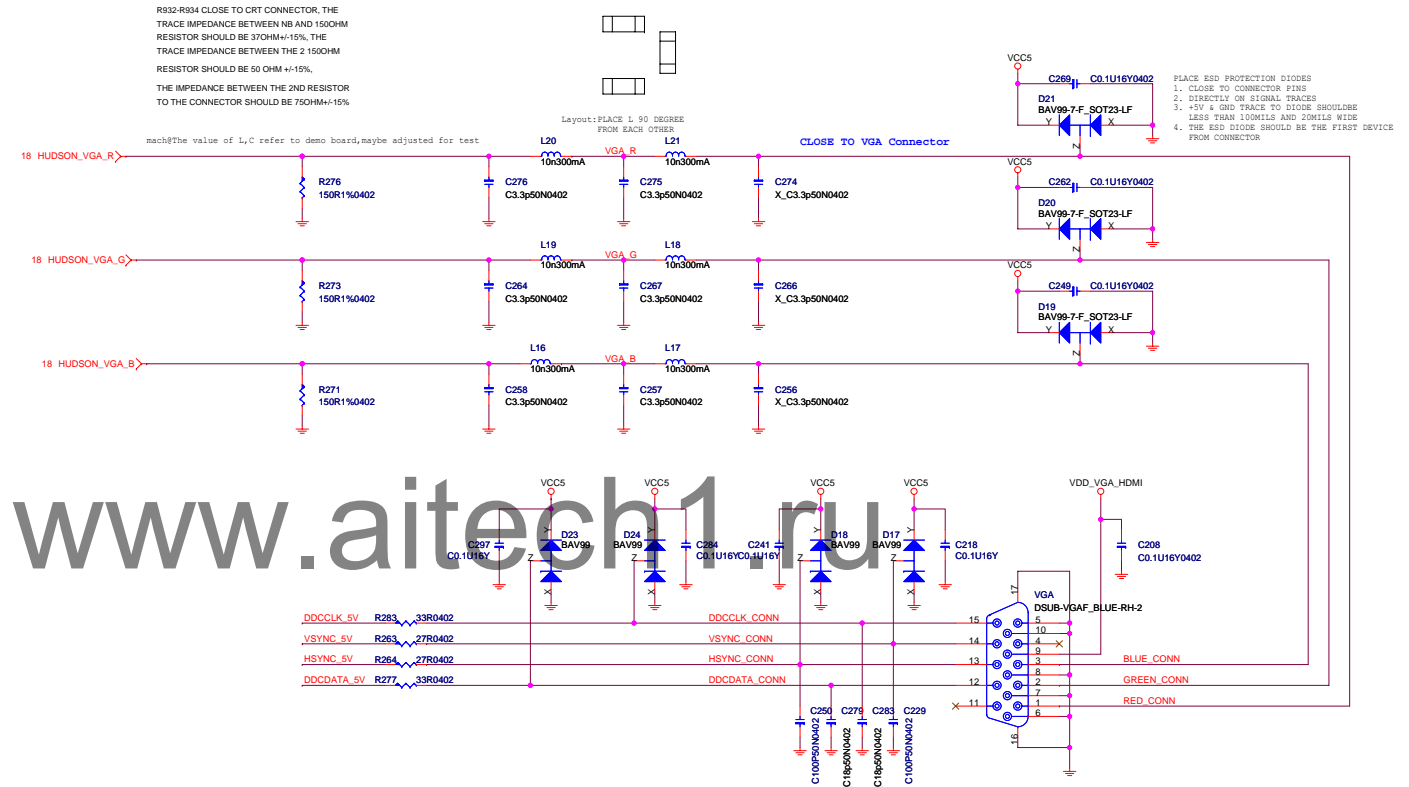
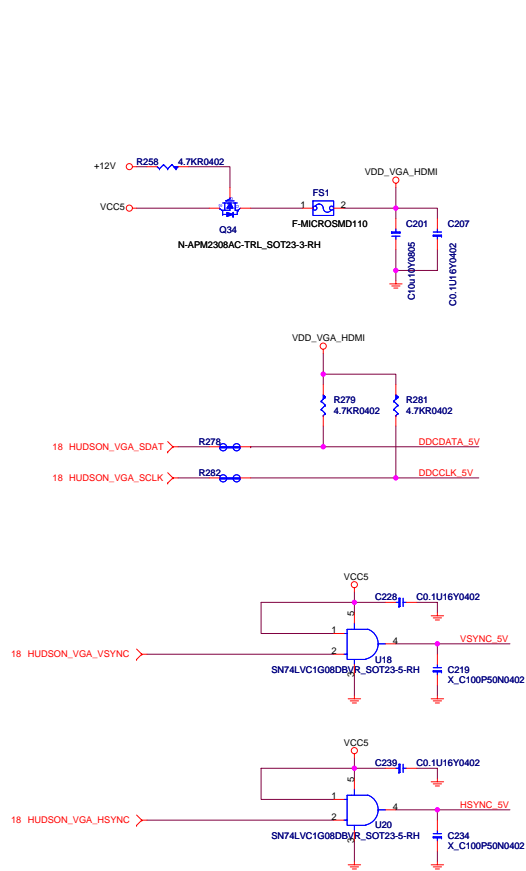
DP CONFIGURATION TABLE				
INTERFACE	DP PORT OF PM1			
DP	3	2	1	0
HDMI	Channel1Clock	Ch 0	Ch 1	Ch 2



www.aitech1.ru



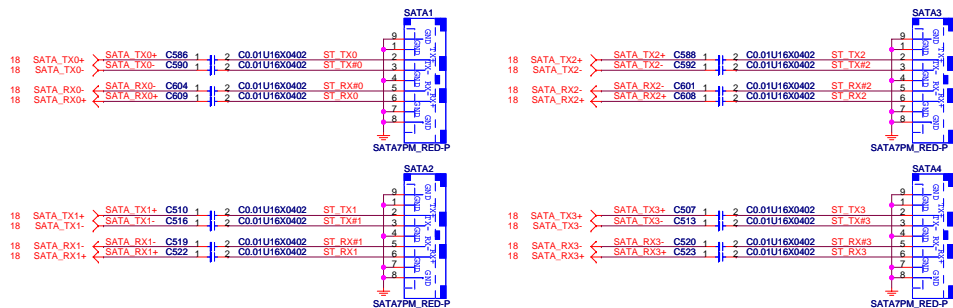
VGA CONNECTOR



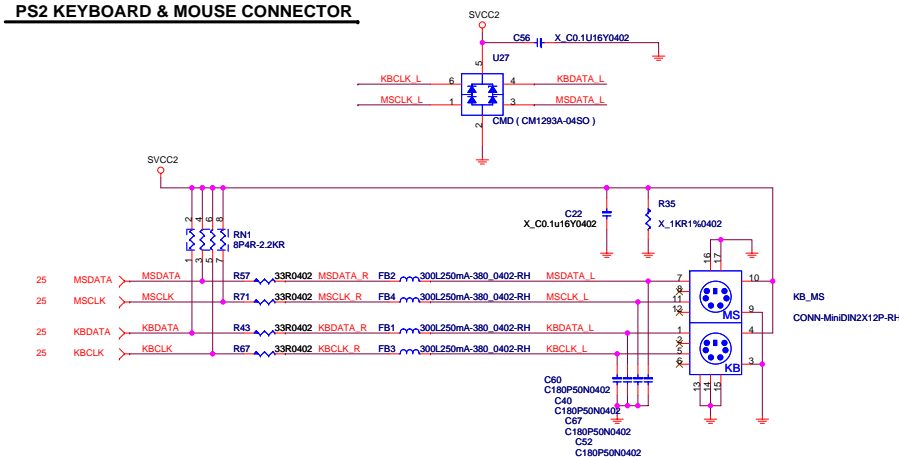
- PLACE ESD PROTECTION DIODES
1. CLOSE TO CONNECTOR PINS
 2. DIRECTLY ON SIGNAL TRACES
 3. +5V GND TRACE TO DIODE SHOULD BE LESS THAN 100MILS AND 20MILS WIDE
 4. THE ESD DIODE SHOULD BE THE FIRST DEVICE FROM CONNECTOR

Multiple eSATA function

Layout: For Gen 3.0, trace length within 3''

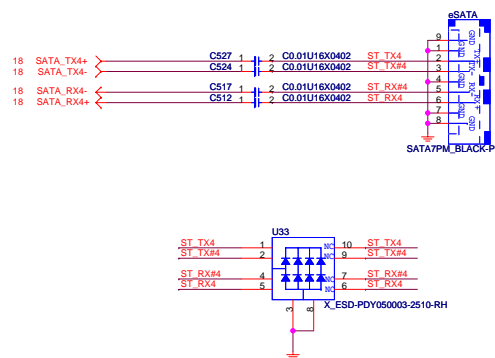


PS2 KEYBOARD & MOUSE CONNECTOR



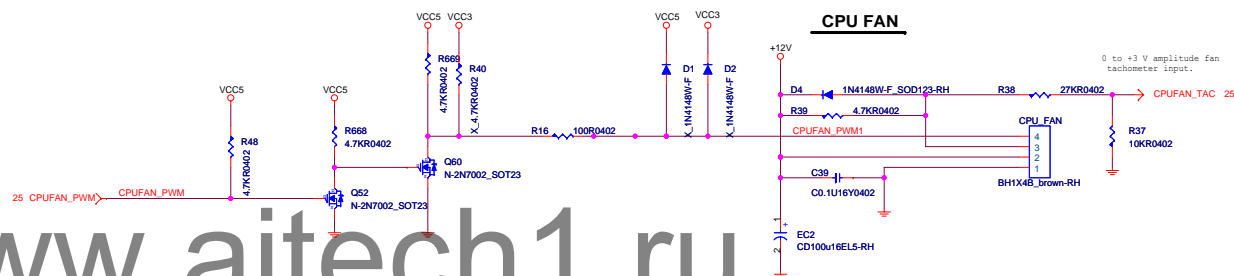
eSATA Conn. WO re-driver

Layout: For onboard eSATA conn. without redriver IC, trace length within 6"

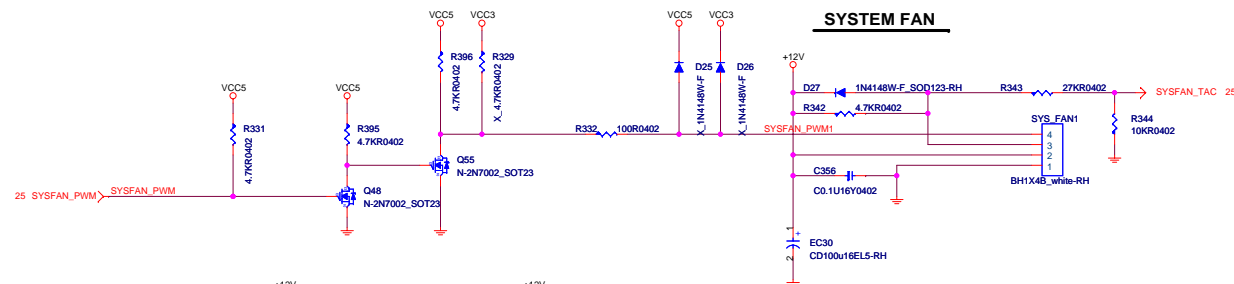


PWM FAN CONTROL

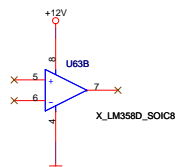
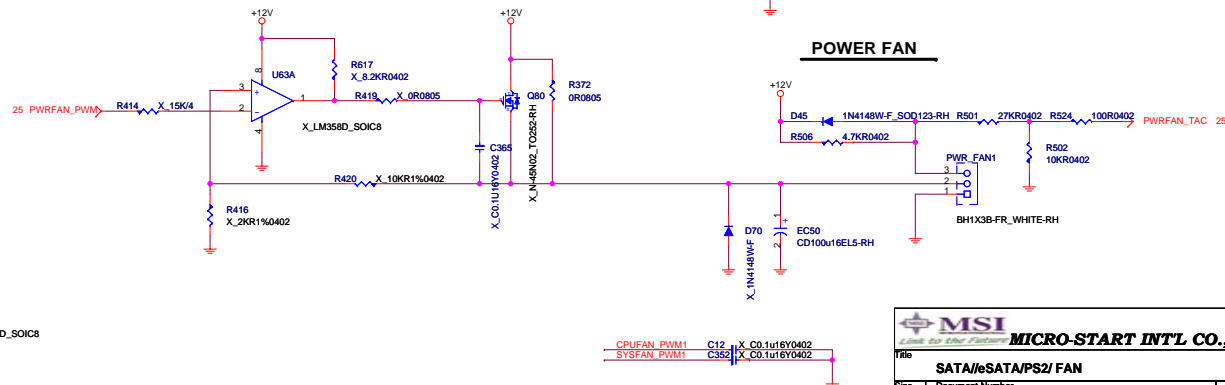
CPU FAN



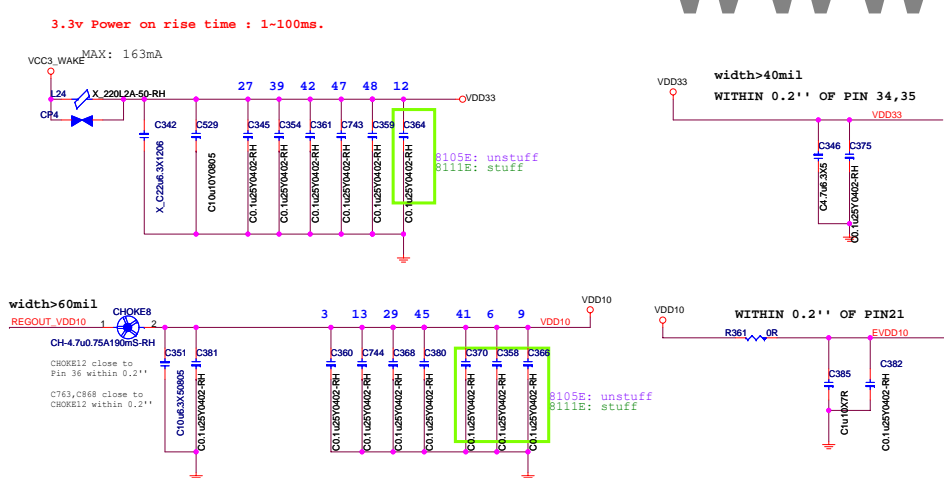
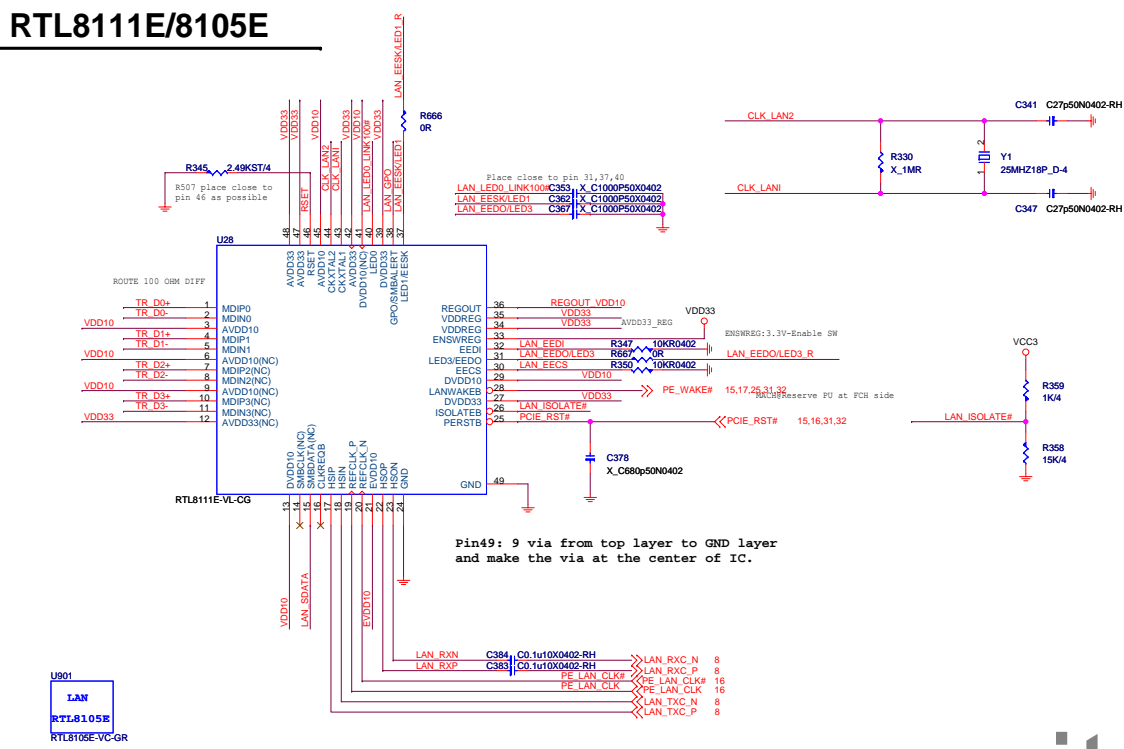
SYSTEM FAN



POWER FAN



RTL8111E/8105E



8105E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	14/75	46/248
100 M Idle/TxRx	43/66	142/218
S0 ALDPS	3.2	11

8111E POWER Consumption

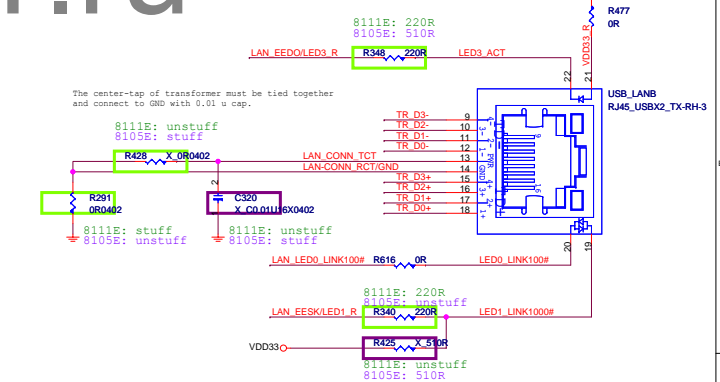
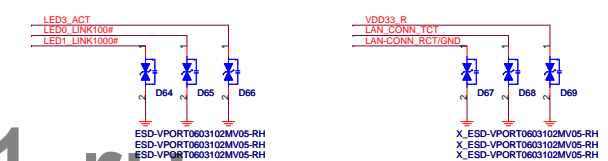
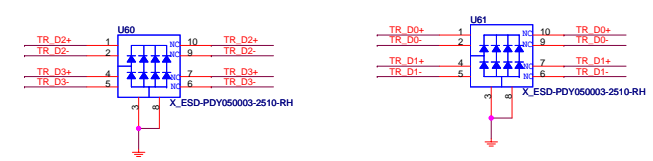
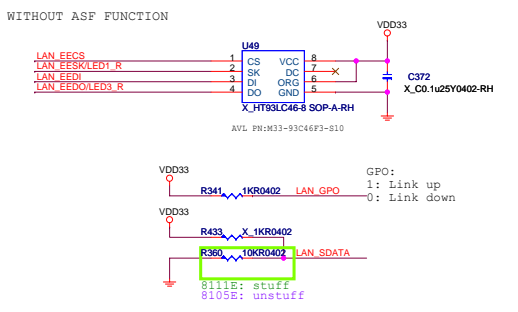
	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13

N58-22F0431-U30 (10/100)

WOL	status	Yellow	Gm/Org
don't care	No Link	off	off
off	S3/S4/S5	off	off
on	S3/S4/S5	off	off
on	10M.inactive		off
on	10M.active		off
on	100M.inactive		
on	100M.active		
on	1G.inactive		
on	1G.active		

always on
always on
always on
blinking

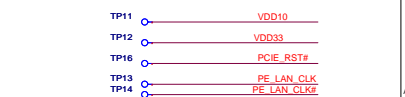
USE Efuse/BIOS PATCH WITHOUT ASF FUNCTION

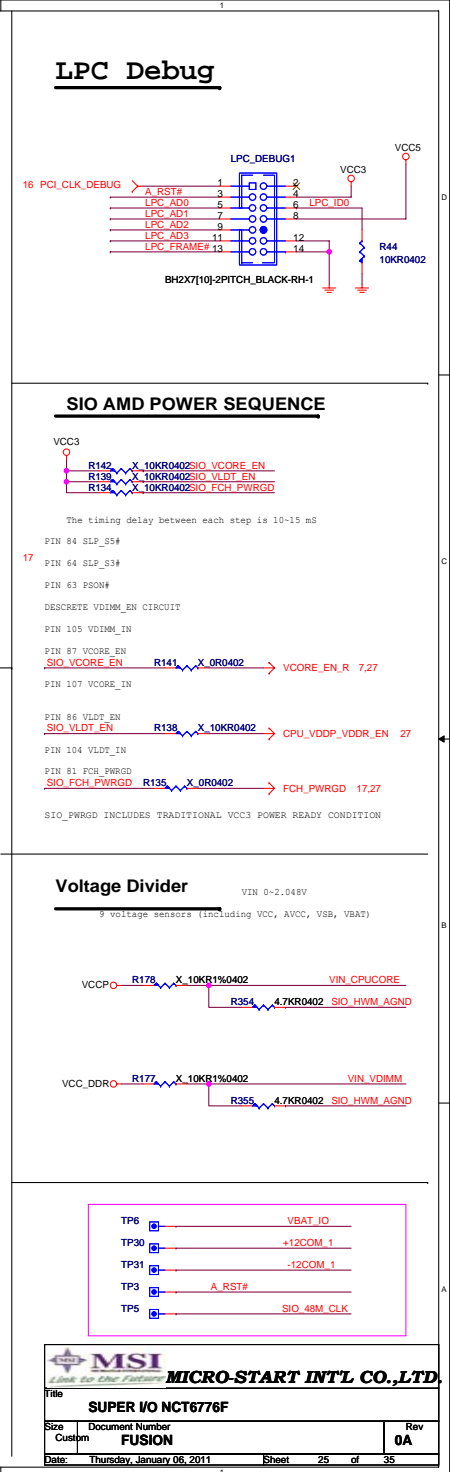


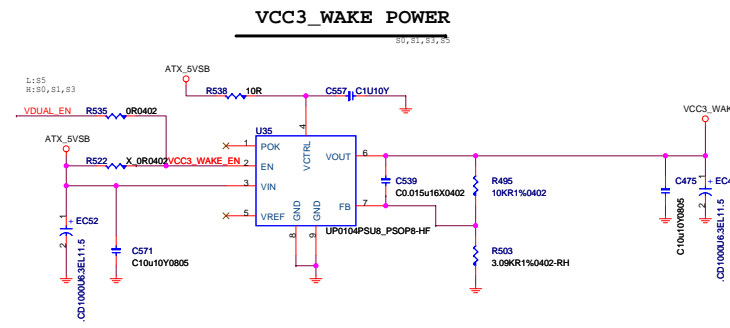
N58-22F0951-I60 / N58-22F0431-U30

Giga-Lan	10/100-Lan
Link Yellow	Link Yellow
Active Blinking 1000	Active Blinking 100
Green 100	Green 10
None 10	None
19	19
20	20
21	21
22	22

only support LED0+LED1/LED1+LED3 dual color LED combinations when using EEPROM





[illegible]

SVDIMM FOR DDR

VCC5

ATX_5VSB

5,25,27,33 ATX_PWROK

R293 510R0402

5VDDIMM 5V

R298 10R0402

ATX_5VSB

R298 10R0402

C309 X_C0.1u16Y0402

C325 X_C0.1u16Y0402

U23

5VSB_DRV

5VSBDRV1

C212 C18000p16X0402

Q47 P06P03LCQ_S0T89

5VDDIMM

17,25,27,30 SLP_S3#

17,25,27,30 SLP_S5#

ATX_5VSB

R299 X_4.7K0402

MODE 4

R295 0R0402

MODE 4

5VCC_DRV

5VDRV1

UP7501M8_S0T23-8-RH

R284 1.5K-RH

C294 C0.022u250X

C296 200K0402

Q46 N-45N02_2052-RH

VCC5

5VDRV1_EN

CRB: MODE Low support S0/S3
Hi support S0/S3/S5

For special PSU sequence

VCC3

ATX_5VSB

R323 X_1K0402

R306 X_47K01%0402-RH

5VDDIMM 5V

R322 X_4.7K0402

Q50 X_N-2N7002_S0T23

C333 X_C0.1u16Y0402

Q51 X_N-2N7002_S0T23

[illegible]

The circuit diagram shows the VCC3_ALW power supply regulation. It features a U37 UPD111AMA5-00, SOT23-6-HF voltage detector. The VIN pin is connected to C558 (10µF) and C555 (10µF). The VOUT pin is connected to a network of resistors R512 (3.16K), R513 (1KR), and R514 (1KR), along with capacitors C556 (10µF) and C563 (10µF). The EN pin is connected to GND. The FB pin is connected to a 0.8V reference. The output is labeled VCC3_ALW.

$$P_{dr} = (V_{in} - V_{out}) \times I_{max} = (5 - 2.5) \text{ V} \times 0.2 \text{ Amp} = 0.5 \text{ W}$$

$$I_{on} = 0.8 \times (R1 + R2) / R1$$
[illegible]

1.1VDUAL POWER

1.V@1.3A----D3
0.6A----D2

VB VCC1P1

NB VCC1P1

SVDVRV1

+1.1VDUAL

EC47

C2D00u16EL5-RH

C525 C10u10Y0805

EC71

+VIN U55

R498 0R0402

R496 10R

VCC5_SB

U55 UP0104PSU8_PSOP8-HF

EN 2

VIN 3

VREF 5

GND 4

GND 6

FB 7

VOUT 8

0.8 V

PDR=1.9W

Vor=0.8*(R1+R2)/R1

R2 1KR1%0402

R499 1KR1%0402

R583 200KR0402

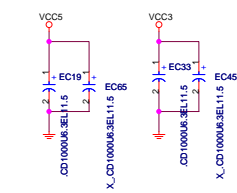
R479 2.61KR1%0402

SVDVRV1

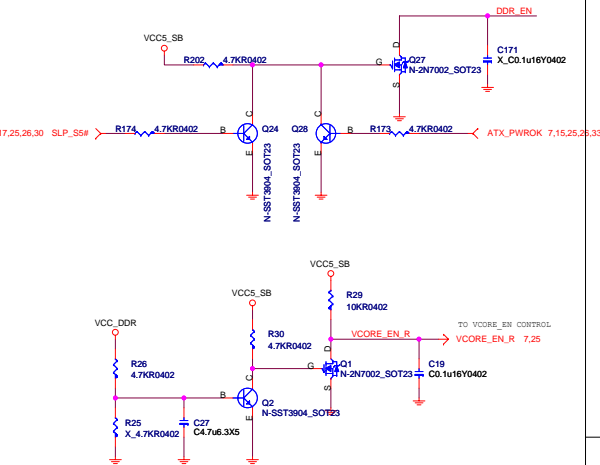
C783 C0.015u16X0402

C528 C10Y0805

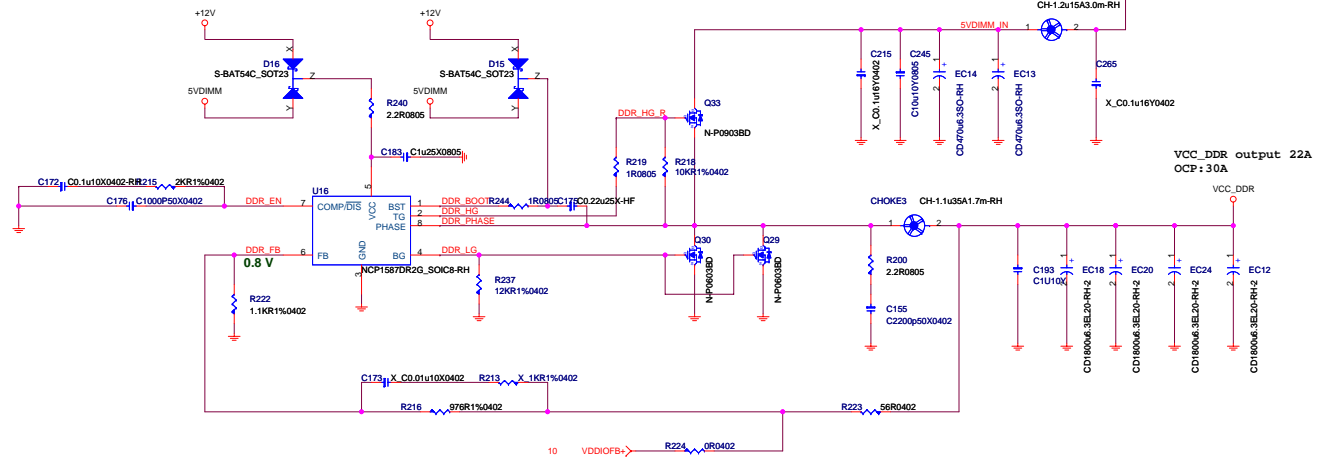
Formula: $P_{dr} = (V_{in} - V_{out}) \cdot I_{max} = (3.3 - 1.1) \text{ V} \cdot I_{BD} \text{ Amp}$



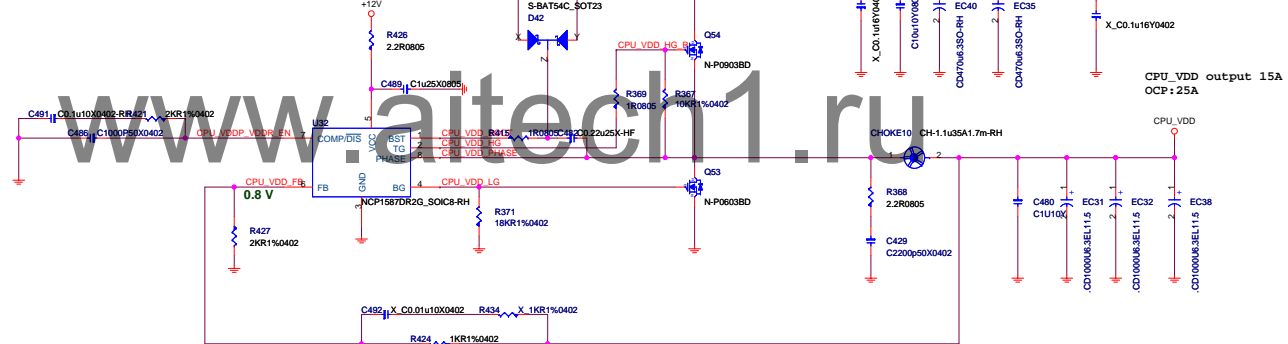
POWER EN & PWRGD LOGIC CIRCUIT



DDR III 1.5V POWER

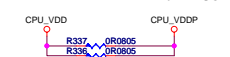


CPU VDD POWER



VDDP and VDDR support two separate power planes with single regulator

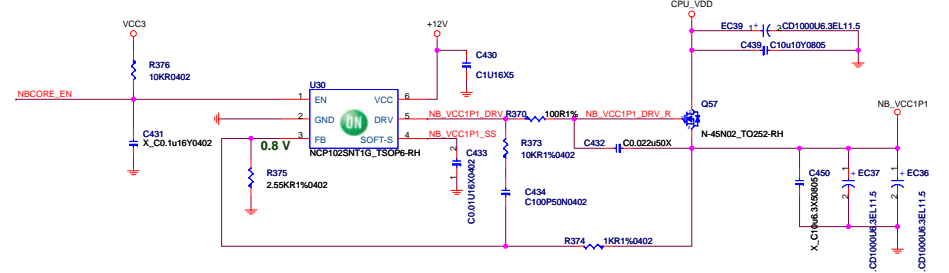
CPU_VDDP POWER 1.2 V@5A



CPU_VDDR POWER 1.2 V@5A



NB VCC1P1 POWER



Link to One Fusion			
MICRO-START INT'L CO.,LTD			
FCH CORE & DDR Power			
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NEAR USB CONNECTOR

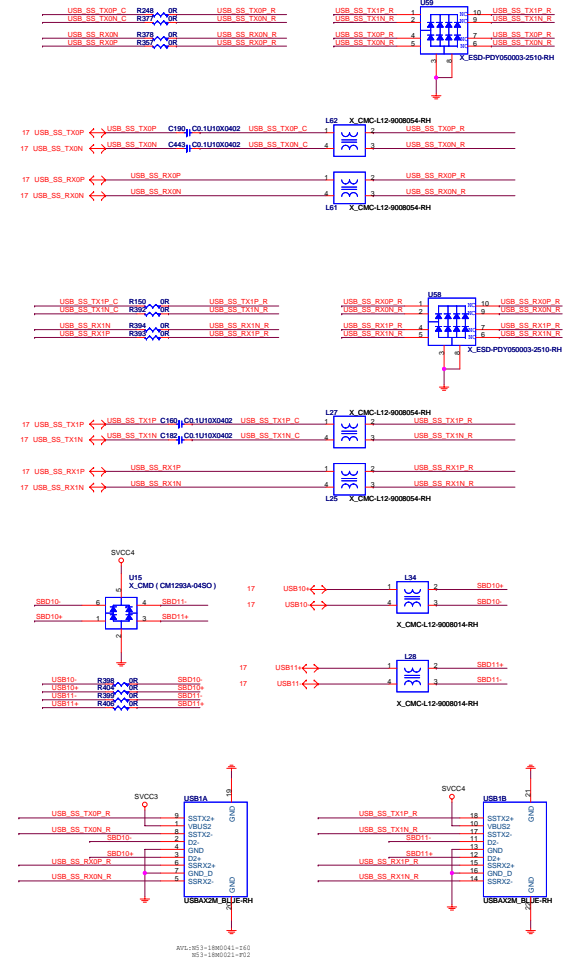
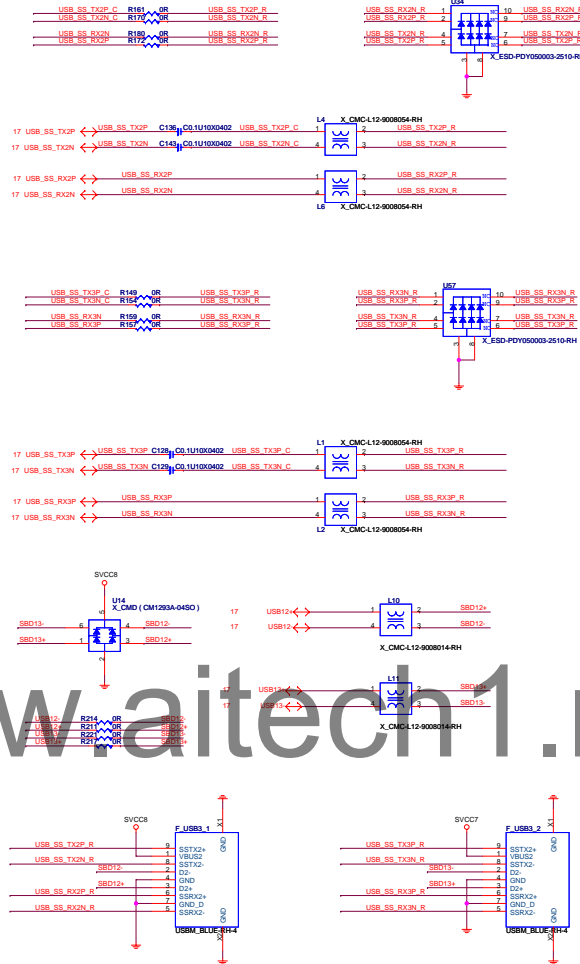
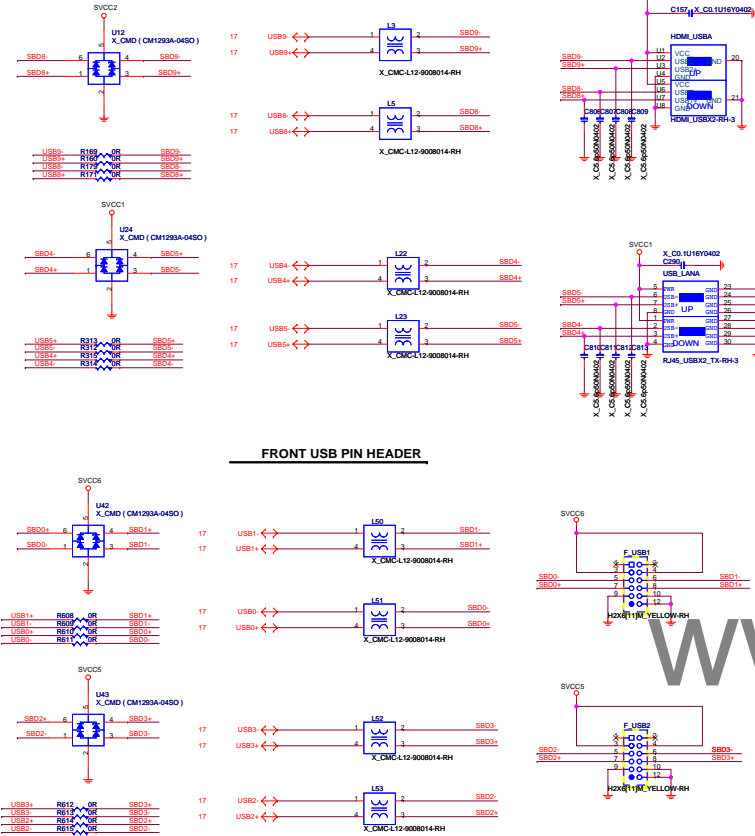
REAR PANEL USB CONNECTOR

FRONT USB PIN HEADER

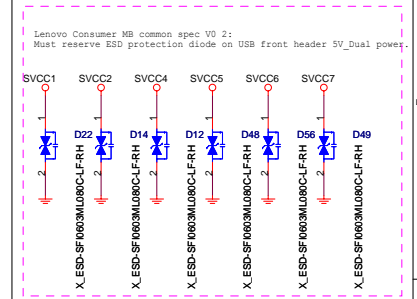
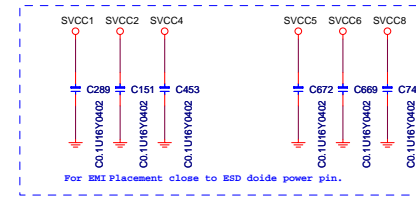
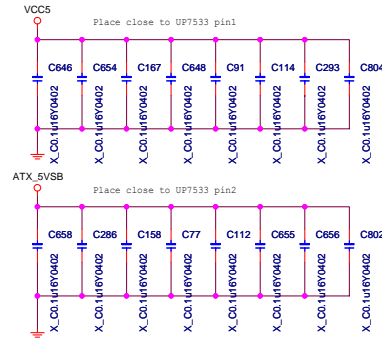
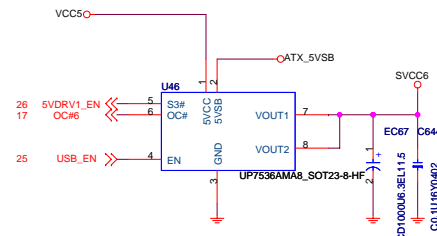
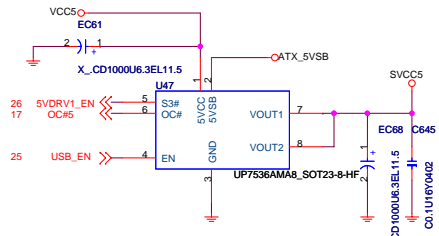
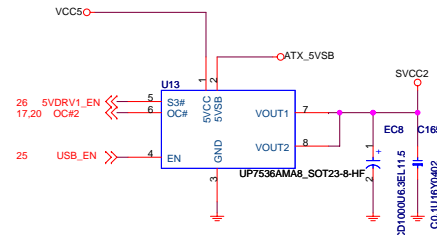
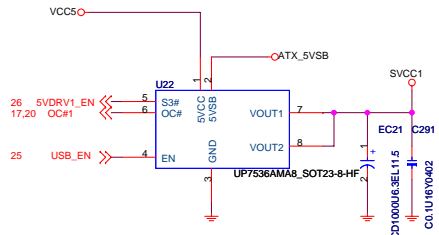
USB 2.0 trace length
REAR side within 18'';
FRONT side within 6''

USB 3.0 trace length
Front pin header within 3.5''

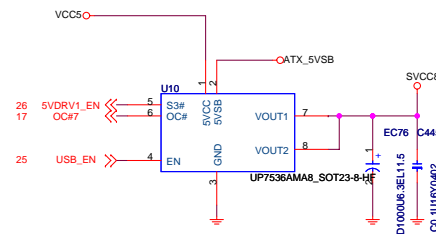
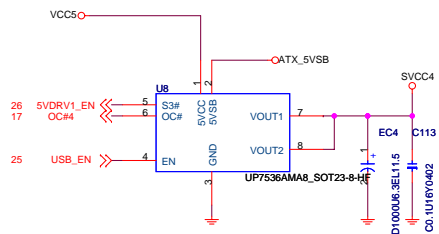
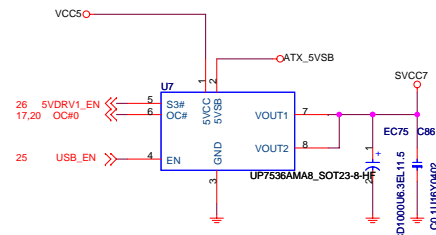
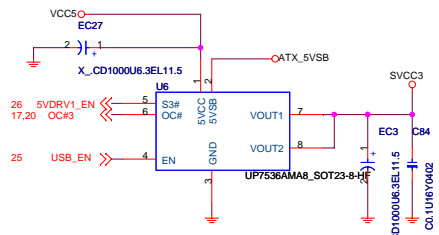
USB 3.0 trace length
Rear connector within 8''



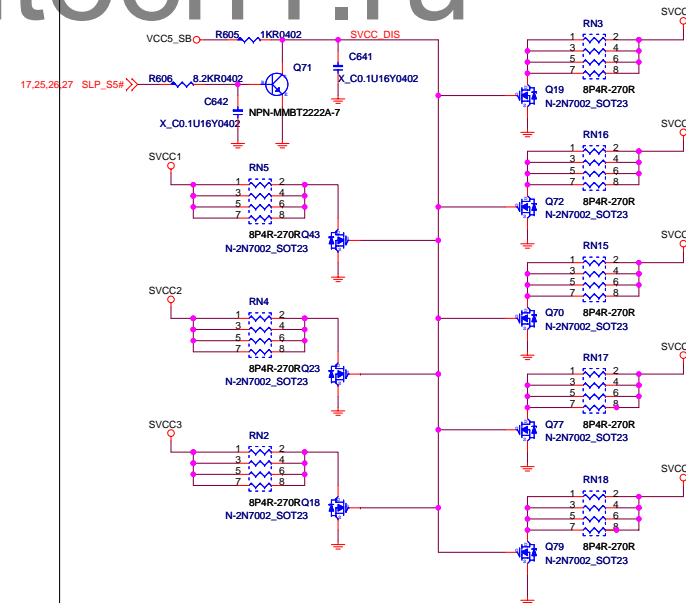
USB 2.0 0.5A pert port



USB 3.0 0.9A pert port



USB power discharge circuit



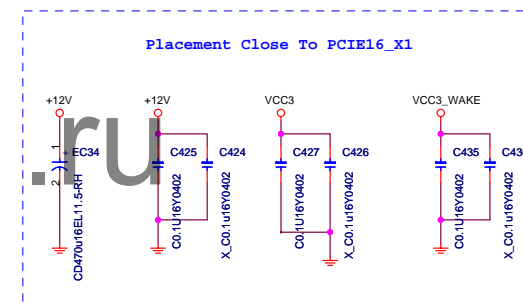
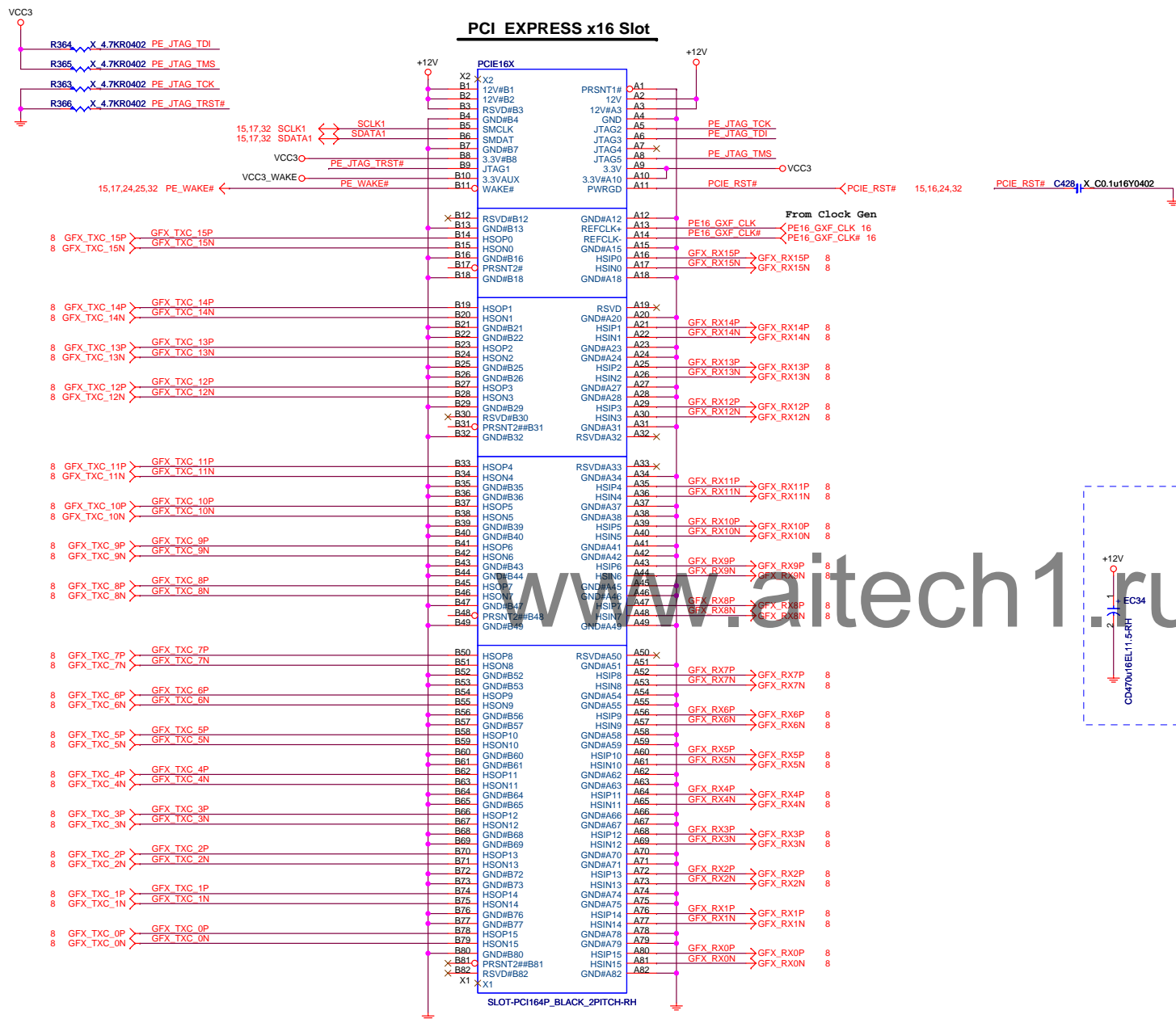
Use low-pass filter to prevent glitches during plug/unplug events.

OC#0 C111 C0.1U16V0402
OC#1 C96 C0.1U16V0402
OC#2 C116 C0.1U16V0402
OC#3 C132 C0.1U16V0402
OC#4 C141 C0.1U16V0402
OC#5 C603 C0.1U16V0402
OC#6 C748 C0.1U16V0402
OC#7 C749 C0.1U16V0402

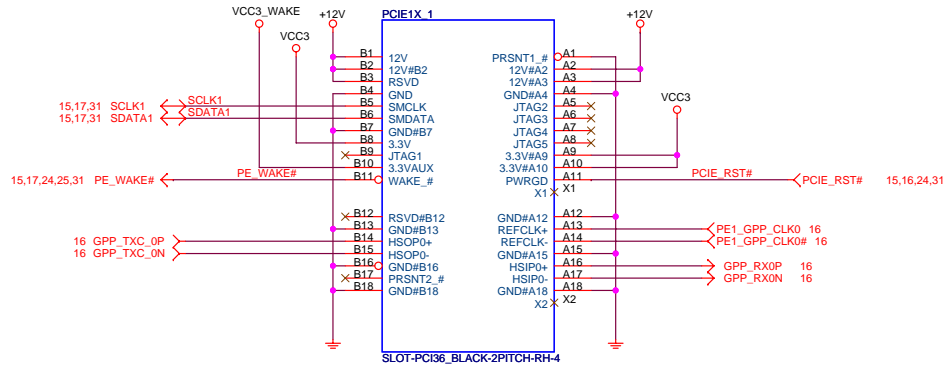
MSI
Link to the Future
MICRO-START INTL CO., LTD.

USB POWER/DISCHARGE			
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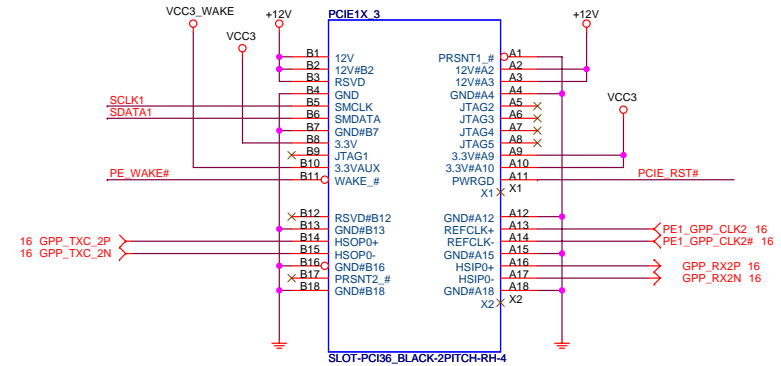
PCI Express Slot x16



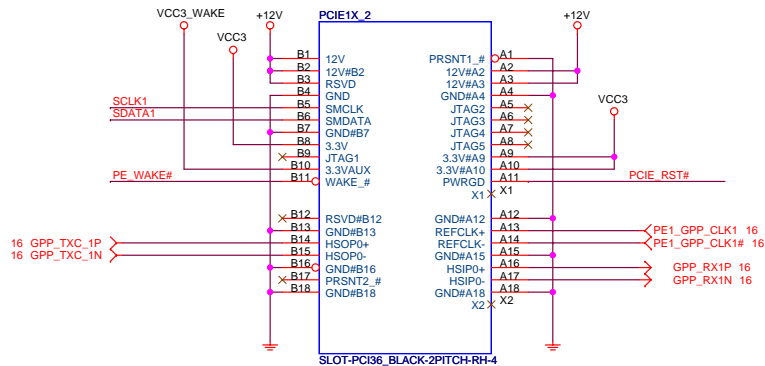
PCI EXPRESS X1 Slot-1



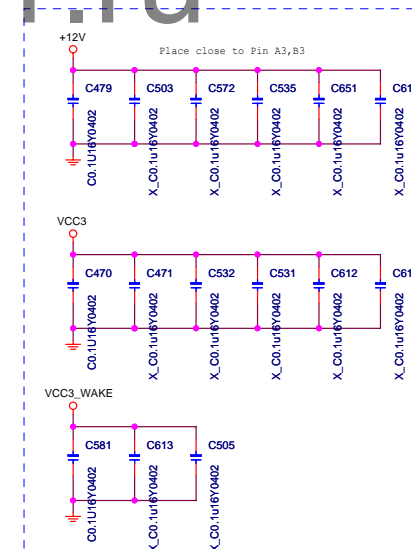
PCI EXPRESS X1 Slot-3



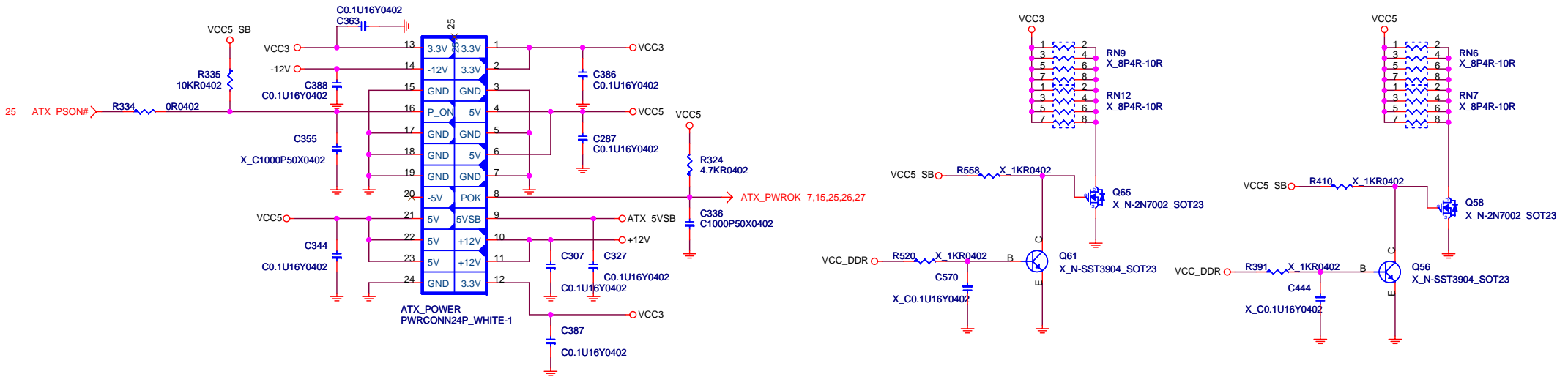
PCI EXPRESS X1 Slot-2



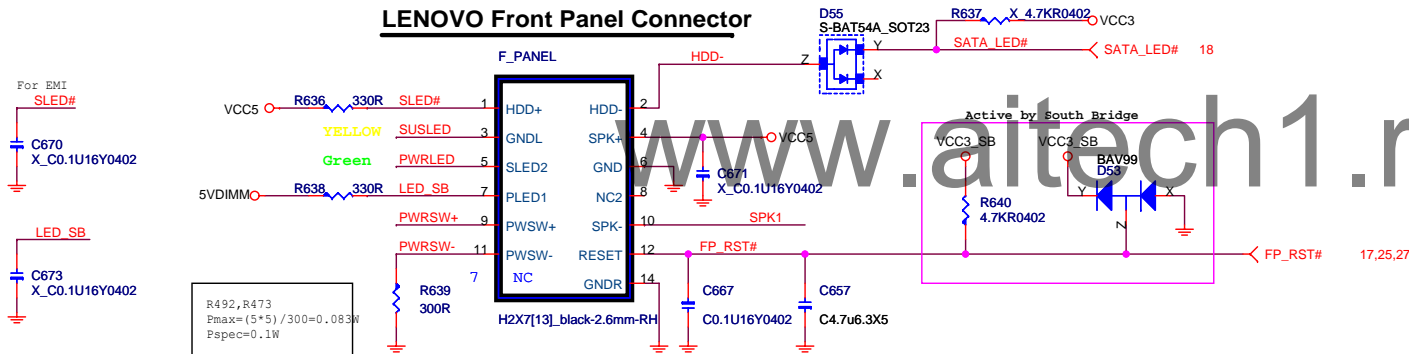
PCIE_RST# C472 X_C0.1u16Y0402



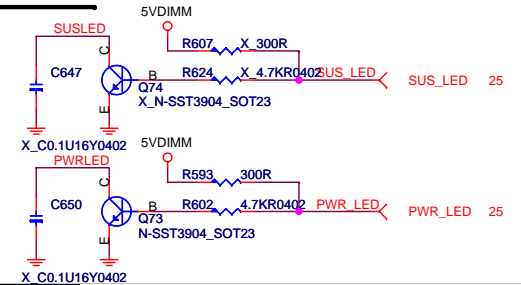
ATX CONNECTOR



LENOVO Front Panel Connector



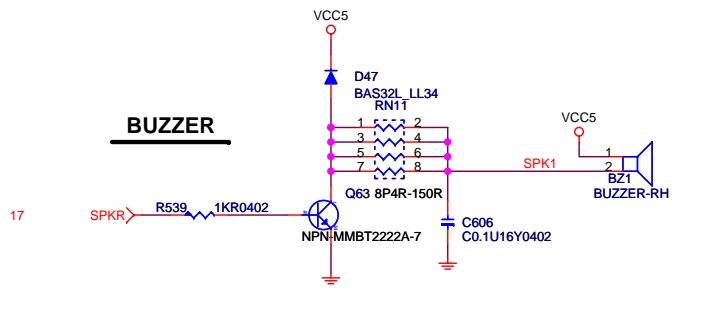
POWER LED



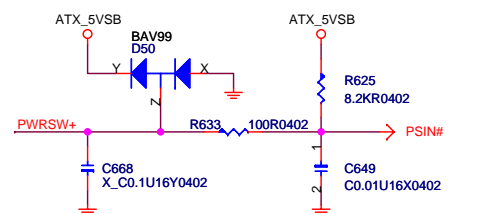
power LED definition

HD (IDE Hard Disk Active LED)	
Pin 1: LED anode(+)	Pin 8: LED cathode(-)
(Power LED)	
Power Switch	Pin 3: LED cathode(-) (green)
	Pin 2: LED cathode(-) (yellow)
LED Status (Dual color LED)	
System State	Dual Color POWER LED State
S0	Steady Green
S1	Green Blinking (frequency is under 1Hz)
S3	Steady Yellow
S4/S5	Off
Default S5 in lose power. Note series resistor is 330Ω	

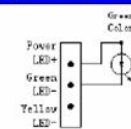
BUZZER



POWER BUTTON

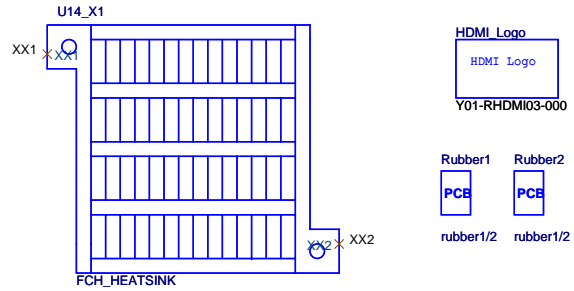


2-pin single color Power LED

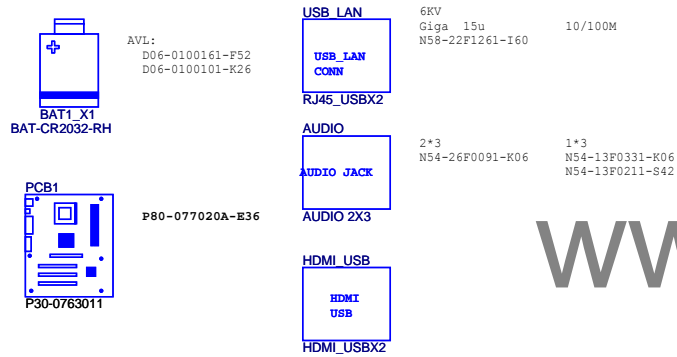


MICRO-START INT'L CO.,LTD.		
Title		
ATX & FRONT PANEL		
Size B	Document Number	Rev
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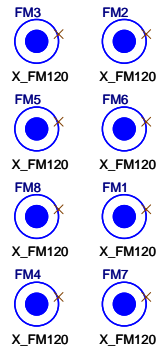
HEAT SINK



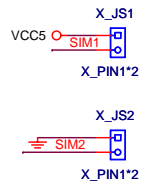
MANUAL PART



Optics Orientation Holes



Simulation



Pangkor

